ClockDistribution/TriggerTimestamping in CTA - an Update

The task:

1. Distribute a precision clock to all telescopes (PPS .. signals)
2. Timestamp each camera trigger + distribute to DAQ center

A subtopic of ACTL-TRIG WG (+ ArrayTrigger)

Ralf Wischnewski + WR team (DESY/UVA/HUB)

Zeuthen, 20141008

CTA going for a (unique) White Rabbit

Downselection Process finished in 8/2014

1. White Rabbit (WR) chosen versus Mutin (APC)
   - official: both WR and Mutin “are well developed”, only a (minor) manpower issue @APC.

2. WR concept decided (being the DESY all-camera WR-proposal from 2012):

   - Same WR-components & standard camera interface for all xSTs

   - Brings SSTs on-board (Amsterdam), before with custom/expensive solution
   - Functionality:
     - Clock to Camera
     - Trigger from Camera is timestamped
   - Catania-news: FlashCam refuses sending trigger (it’s CTA...) (“FlashCam will do all itself”)

CTA going for a (unique) White Rabbit

- WR team is now: DESY / HUB / VUAmsterdam (D.Berge, A.Balzer)
  other groups joining ?

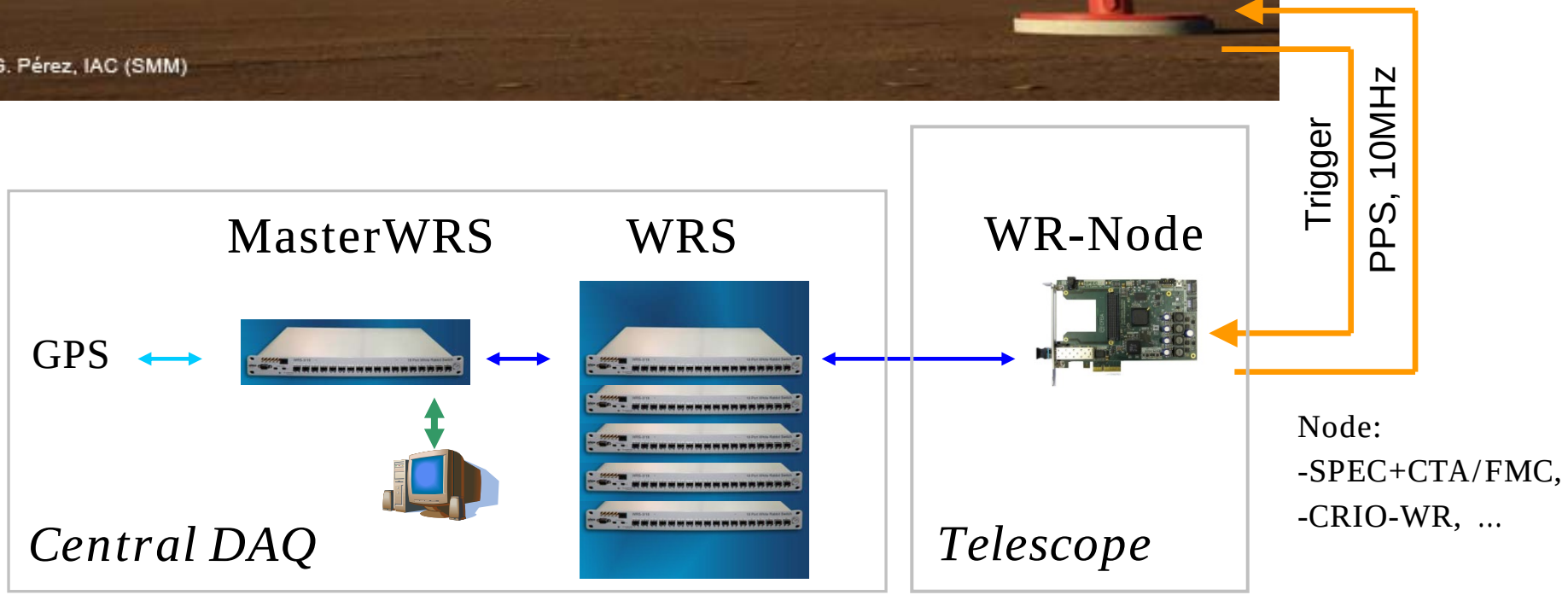
- Camera IF discussion intensified
  - MST/LST: Camera bulk data content (redundancy, camera-time)
    Event header (w/ time/trigger type)
  - Events-wise deadtime /vetoed events
  - ...

- TDR - WR section in final phase
- DESY resource planning

- Data flow: TimeStamps to → ArrayTrigger (SWAT) and/or → CamServer
- Concept for
  - Redundancy
  - Field-work: Calibration, Commissioning, Debugging
  - Pre-installation tests

WR in CTA: in a nutshell

WR-Workshop,
CERN/20141006

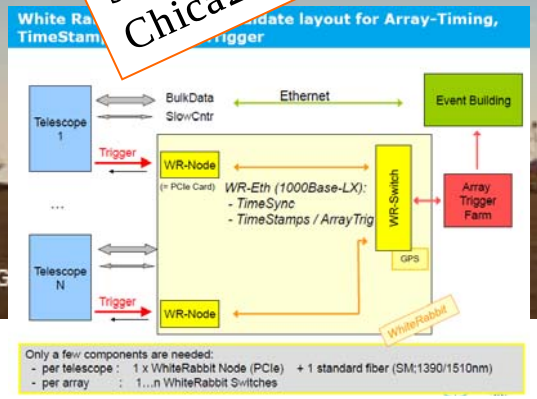


Node:
-SPEC+CTA/FMC,
-CRIO-WR, ...

WR in CTA: in a nutshell

WR-Workshop, CERN/20141006

see DESY Proposal Rome2012; Chica2013; ACTL 2012



MasterWRS

WRS

WR-Node

GPS

Trigger

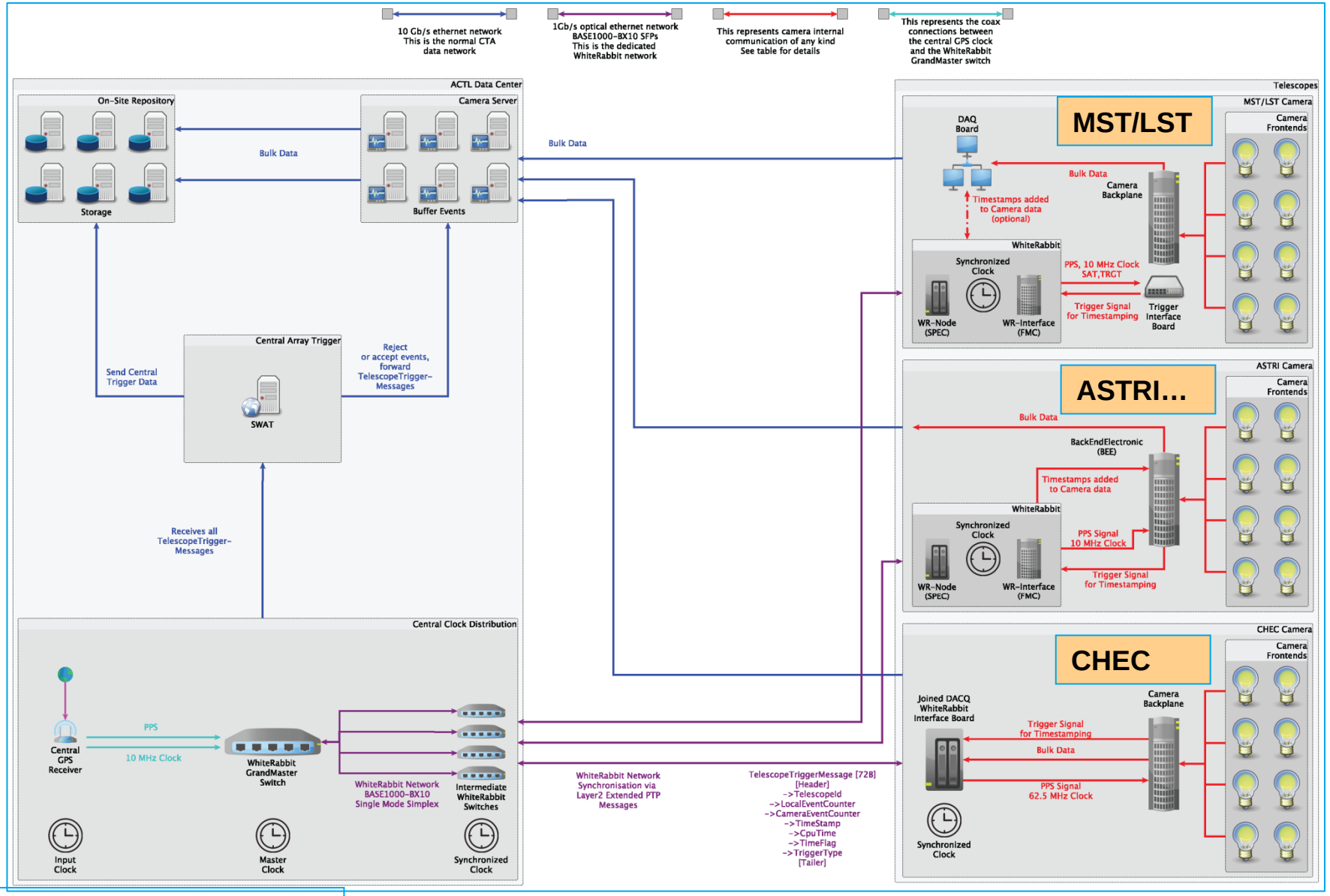
PPS, 10MHz

Node:
-SPEC+CTA/FMC,
-CRIO-WR, ...

Central DAQ

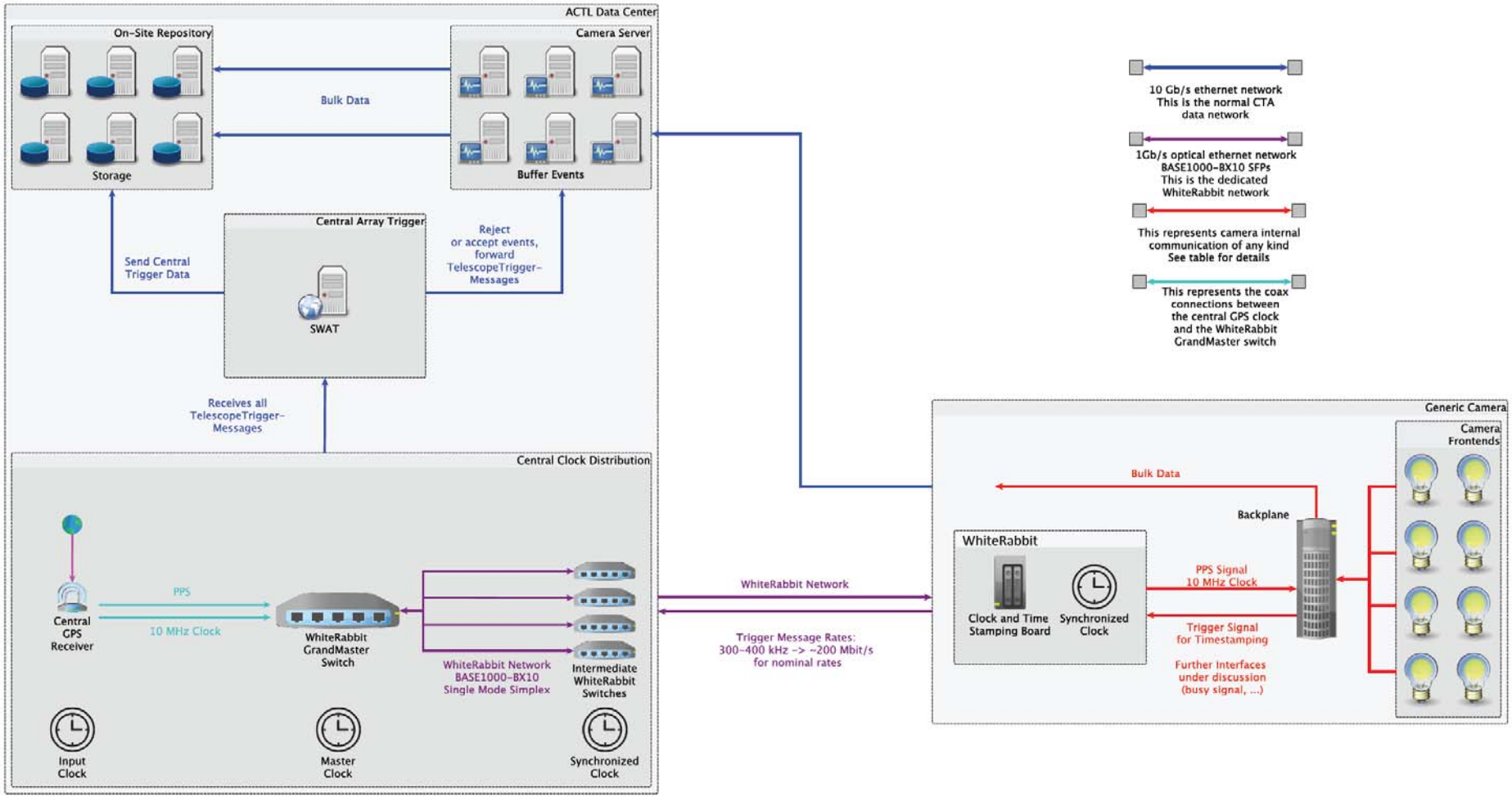
Telescope

WR in CTA - The concept as of July-2014



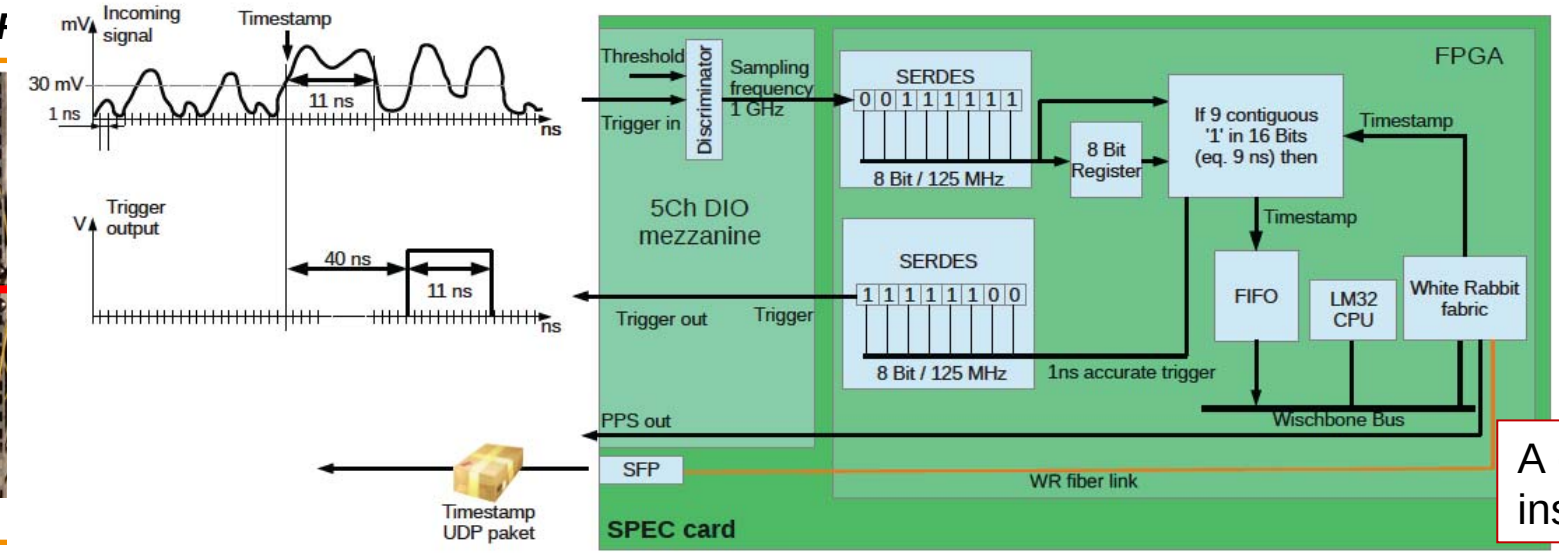
From redmine-ACTL wiki)

WR in CTA - The unified concept September-2014



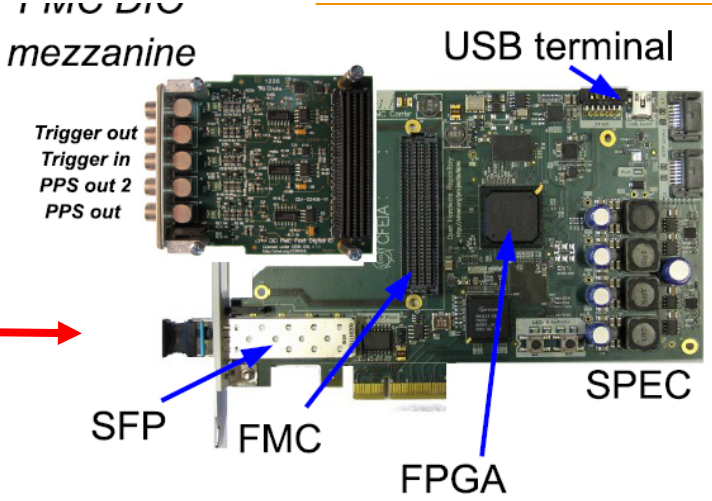
(SST: CHEC/DigCam now joind the standard interface concept)

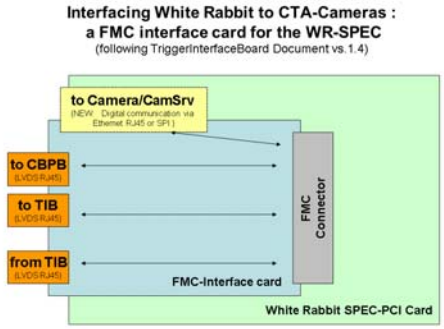
WR – SPEC : Adapt the FPGA to CTA requirements



A glimpse inside the SPEC

Figure 3: The modified FPGA architecture of the SPEC card for timestamping and evaluating incoming signals. The left side shows an incoming signal and the resulting output trigger signal after a constant delay of 40 ns.



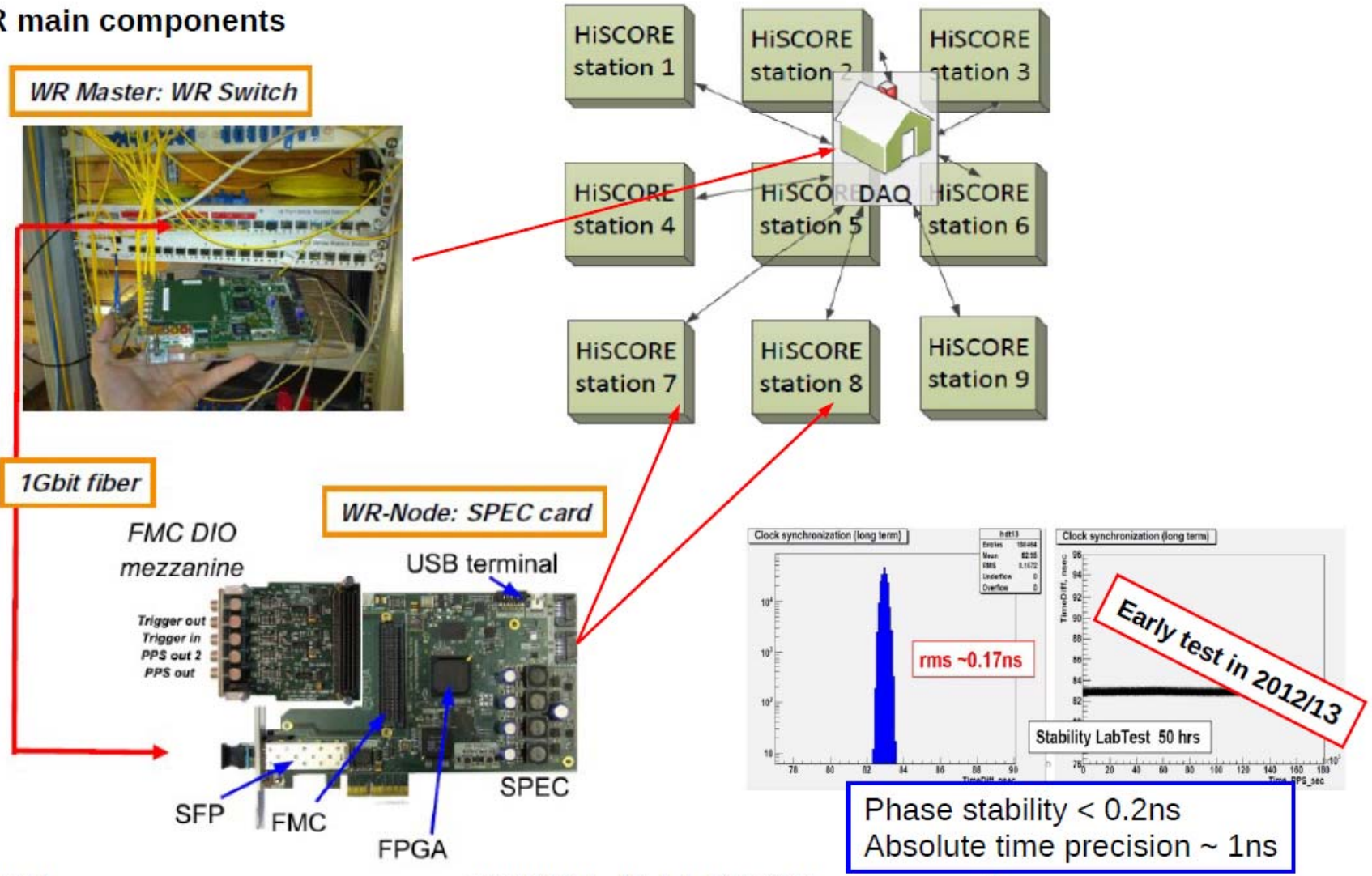


Adapted the SPEC-FPGA to
- Time stamping
- trigger logic
- UDP data transport

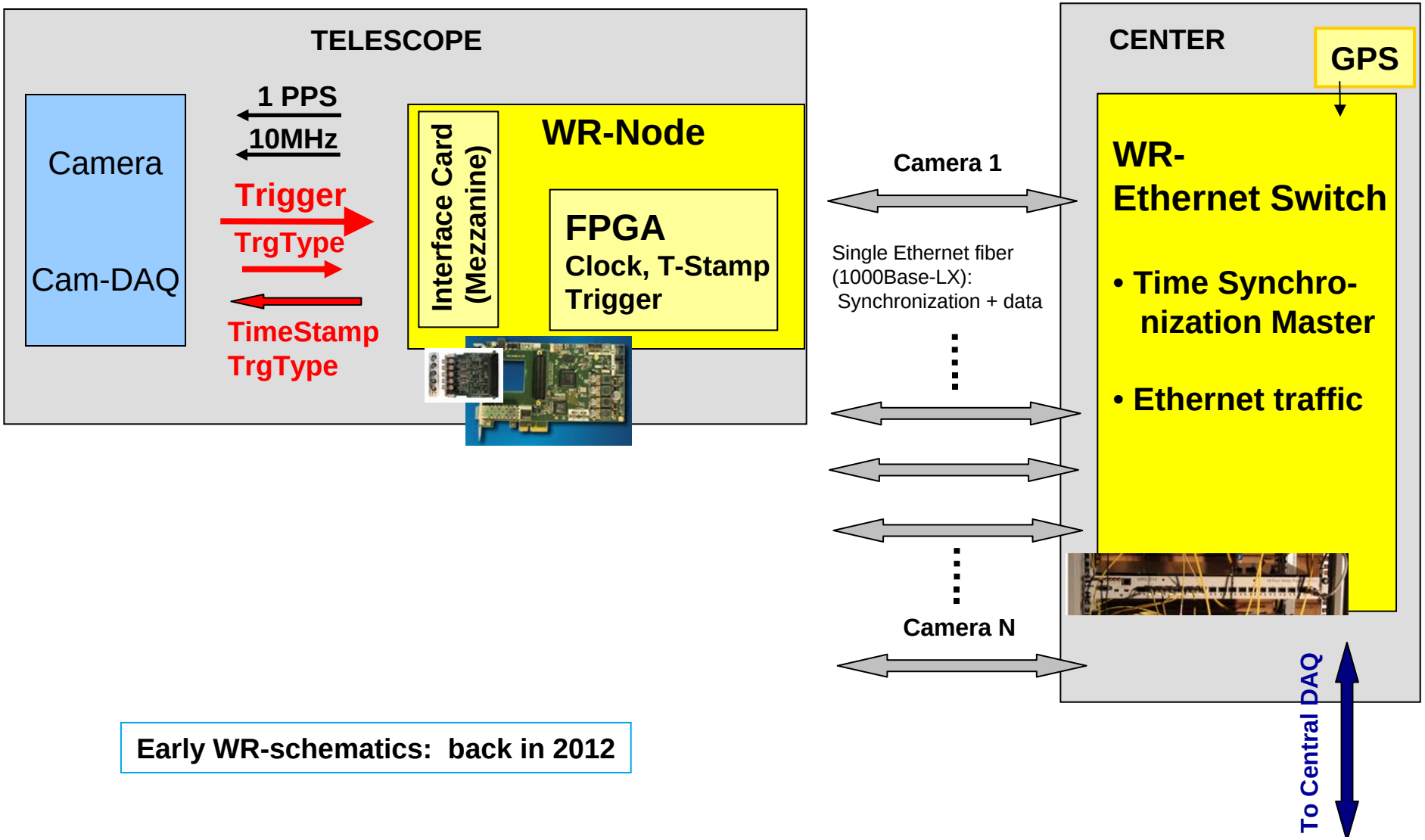
The CTA WR-SPEC Interface card. Work in progress.

WhiteRabbit timing system

- **WR main components**



White Rabbit at CTA: Baseline architecture



Early WR-schematics: back in 2012