33RD INTERNATIONAL COSMIC RAY CONFERENCE, RIO DE JANEIRO 2013
THE ASTROPARTICLE PHYSICS CONFERENCE

ICRC 2013

A White Rabbit setup for sub-nsec synchronization, timestamping and time calibration in large scale astroparticle physics experiments

M.BRÜCKNER[1], R.WISCHNEWSKI[2]

[1] *Department of Computer Science, Humboldt-University Berlin, Rudower Chaussee 25, 12489 Berlin, Germany*
[2] *DESY, Platanenallee 6, 15738 Zeuthen, Germany*

martin.brueckner@informatik.hu-berlin.de, ralf.wischnewski@desy.de

Abstract: Time synchronization with nanosecond precision between individual detectors, distributed over km-scale, is a typical challenge for large astroparticle physics experiments. We adapt the new White Rabbit technology, an Ethernet extension for synchronization, precision time and frequency transfer, to build a prototype system for trigger-time stamping and test-pulse injection for a distributed data acquisition environment. We present our design, and detailed laboratory tests. They prove precision and stability of this new system, now ready for application in next-generation gamma-ray or cosmic-ray experiments like HiSCORE and CTA.

Keywords: Gamma Astronomy, Cosmic Rays, White Rabbit, New Technologies, HiSCORE, CTA.

1 Introduction

Time synchronization to nanosecond precision is a typical task in modern large-scale astroparticle physics experiments, where thousands of data-acquisition (DAQ) stations, located at up to several km's distance have to precisely timestamp incoming sensor signals.

In the past, custom-made solutions required a substantial effort for construction, and detailed performance verfication (like for neutrino cerenkov telescopes, cosmic ray and γ-ray air shower detectors). With the new White Rabbit technolgy for precision time and frequency transfer [1] available, this experimental challenge might have a standard solution.

This paper describes an application of the open source ethernet based White Rabbit technology, which we extended with the possibility of time stamping and smart triggering incoming signals at each detector station. We present results of long-term laboratory and environmental chamber tests, which proof excellent timing performance and stability.

White Rabbit has the potential to become a standard tool in modern particle and astroparticle physics.

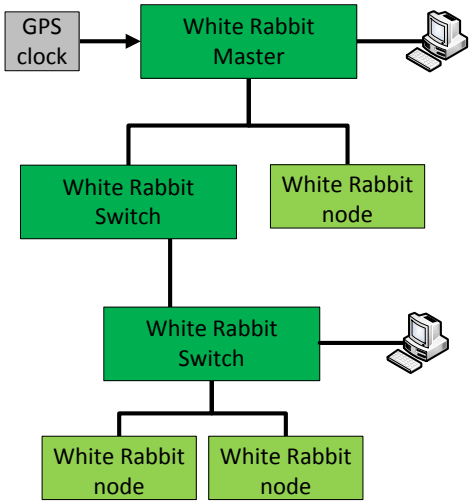

Figure 1: The White Rabbit network

2 White Rabbit

The core technology of the new prototype is the White Rabbit system (WR) [1]. It is a fully deterministic Ethernet-based network for general purpose data transfer and synchronization. WR can synchronize over 1000 nodes with sub-ns accuracy over fiber lengths of up to 10 km. The same fiber is used for synchronization and for standard Gigabit Ethernet packet transportation (see fig. 1). White Rabbit uses the SyncE standard for clock distribution. Additionally, this technology is based on an enhanced version of the Precision Time Protocol (PTP; IEEE1588) to exchange information (absolute time, phase difference, etc.) from the master (the clock distributor) to the nodes [7]. Because of the permanent phase shift correction, White Rabbit can compensate environmental (temperature induced) fluctuations easily. The principle of the clock distribution is that there is a clock master that distributes its clock either directly or via SyncE aware switches to the WR-nodes, see fig. 1

An advantage of the WR system is that the core components are ready to use and ready to adapt to specific WR node functionalities. It is an open source project with access to all information neccessary. This includes the WR-core FPGA design, the hardware schematics and so on. White Rabbit capable hardware is commercially available from several companies [8, 9]. Due to the open source factor the functionality of the FPGA design could be adapted and enhanced for the presented here setup. Furthermore, the big, active and very communicative WR-community has made the White Rabbit system a well debugged and calibrated system. In particular, for high demands on longterm precision and stability, the extensive usage and debugging of the WR-key components make it very reliable. In contrast, for any custom made synchronization/timing system the amount of additional long-term

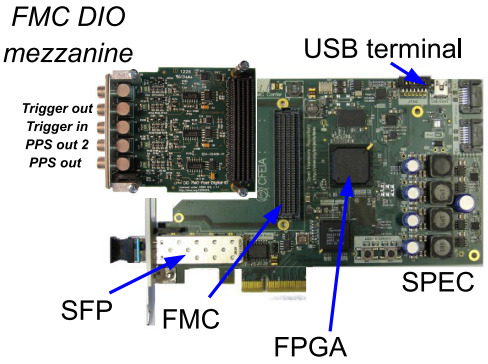

Figure 2: The SPEC card - the White Rabbit node used for this work. The precision time is kept on the FPGA, and synchronized through the fiber cable (SFP connector) to the master clock (see fig. 1).

verification is a huge time and cost factor.

2.1 White Rabbit switch

The key component of the White Rabbit system is the White Rabbit switch. One task of this switch is similar to that of a standard Gigabit Ethernet switch. What makes it special is its possibility to distribute the White Rabbit master clock (or its own clock if the switch is the master clock) over the network. The WRS-3/18 version has 18 SFP connectors.

2.2 SPEC-card and 5Ch DIO mezzanine card

The SPEC (Simple PCIe FMC carrier) card (see fig. 2) is the commonly used White Rabbit node; the White Rabbit FPGA design for this card is well supported. Besides the FPGA (a Spartan-6) there is an SFP connector for the White Rabbit fiber link communication and a USB terminal for timing and status information. The SPEC has a low pin count FMC (FPGA Mezzanine Connector). For the here discussed design, a 5 Channel Digital Input/Output FMC card (DIO5CH) is used and connected to this FMC port. The 5 channels are freely programmable as input or output; for incoming signals a comparator threshold is adjustable. They are used as PPS (Pulse Per Second) output(s), as trigger input or output and as analog signal input in this prototype.

3 Extending the White Rabbit SPEC design

For our new application, the existing White Rabbit SPEC card FPGA design has been modified to extend its functionality.

3.1 Time stamping incoming triggers

Using one channel of the input/output mezzanine card as input for digital ("trigger") signals, it is possible to determine the exact time (relating to the White Rabbit master) with a nanosecond precision. For sampling the incoming signal with a frequency of 1 GHz the on-SPEC Xilinx Spartan-6 FPGA we use the special blocks called "SERDES". They are fast enough to sample the incoming signal with a frequency of up 1050 MHz. With the help of integrated shift registers the FPGA logic can access the digitized signal with a much lower frequency. Due to the 125 MHz White Rabbit clock the register width is 8 bit. An FPGA logic is looking permanentely for bit transitions in this register, i.e. trying to find signal edges. If an edge has been found, the next step is to store the current White Rabbit time in a FIFO connected to the wishbone bus, an internal processor bus. This bus is connected to other White Rabbit components and also to an in-FPGA CPU. To transfer the timestamp information over the White Rabbit link, the CPU software has been modified so that the timestamp FIFO registers are read out and UDP packets are sent to the host PC. The method described is suitable for operating on input signals like digitial trigger signals.

3.2 Triggering analog signals

Instead of operating on digital input signals, derived from external trigger units, the SPEC-DIO5CH comparators can be used to analyze analog signals for a trigger condition with a GHz resolution (e.g. for simple "time-over-threshold" trigger conditions, or more complicated ones). To demonstrate this, a filter was programmed which rejects signals shorter than 9 ns (a value easy to modify). The filter compares the 8 incoming bits together with the previous 8 bits (making it a 16 bit register) parallel with all 16 bit values containing nine contiguous `1` (`0x1FF`, `0x3FE`, `0x7FC`, `0xFF8`, ...).

With this filter it is possible to operate on analog input signals directly and integrate external trigger logic into the WR-card. Thus, the SPEC-DIO5CH becomes an "smart" trigger and timestamping unit. This concept has been successfully applied for airshower triggering and timing for HiSCORE prototype stations [3, 4].

3.3 Trigger output generation

Besides the fact that incoming analog signals are triggered and timestamped, also an output trigger-signal is being generated. To generate a output trigger, precisely aligned to the input signal, it is necessary to conserve the exact position within the 8 bit. Therefore, the original signal is stored in a pipeline and sent to the trigger output port of the mezzanine card if the signal successfully passes the filter. The delay, as shown in figure 3, is 40 ns and does not change or jitter.
With this functionality it is possible to trigger an external measurement unit (e.g. the DRS4 evaluation board [4]) and generate a time stamp only if a valid input signal is arrived.

3.4 Future improvements

Up to now the algorithm implemented in the FPGA for detecting valid incoming signals is very simple. In future more complex algorithms, reconfigurable at runtime, are imaginable. With a FADC adatped onto a custom FMC-mezzanine card, also more advanced algorithms are possible. Another possibility is to run a fourier signal analysis.

For now, the in-FPGA CPU reads the FIFO registers and builds the UDP packets (eg. with time-stamps). This costs much CPU resources, while the main CPU task is to manage the White Rabbit PTP core. Therefore, we plan to make use of the Etherbone concept. Here, the Host PC acts as a Bus Master on the wishbone bus of the SPEC card and polls to FIFO registers by himself, i.e. without utilizing the CPU.

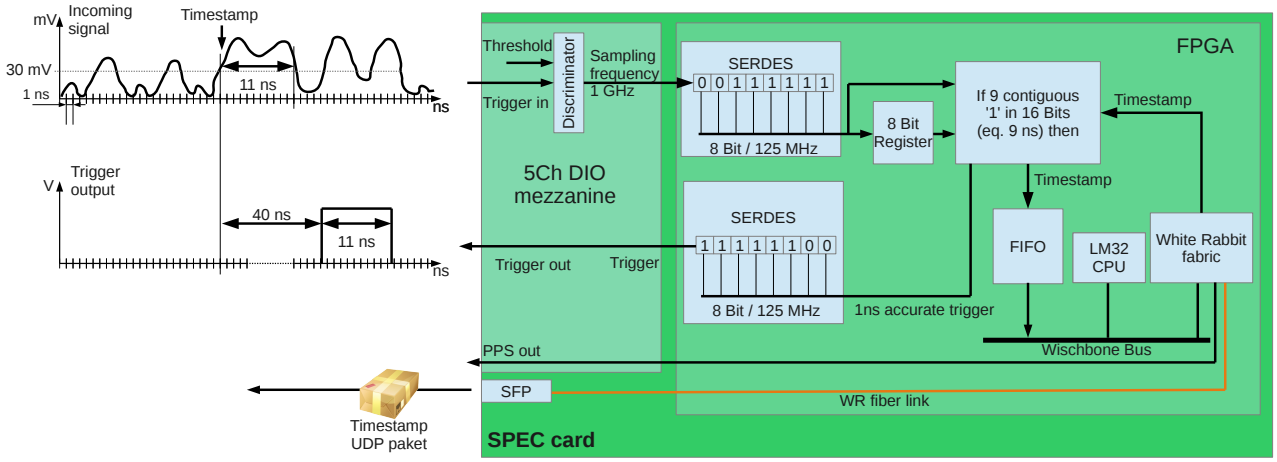

Figure 3: The modified FPGA architecture of the SPEC card for timestamping and evaluating incoming signals. The left side shows an incoming signal and the resulting output trigger signal after a constant delay of 40 ns.

3.5 Laboratory tests

Figure 4 sketches the laboratory setup used to verify stability of the WR-node clocks and the trigger-time stamping mechanism (and the trigger ouput) for two WR-nodes (SPEC1 and SPEC2). Both are synchronized by the WR-switch, which in turn connects to a desktop PC that receives the trigger time stamps from the nodes (UDP-packets), and loggs the SPEC-status (SPEC-USB, not shown). A pulser generates trigger pulses at ∼1 Hz, on purpose asynchronous to the White Rabbit system. Both SPEC cards receive the signal over cables of fixed length, timestamp it internally and send the times over WR-Ethernet to the host. They also generate the trigger output signal (in phase with the local node-clocks). Both trigger-out signals are fed to an DRS4-EB-board (DRS4-2) sampling at 5 GHz. The relative clock phase of the two WR-nodes is measured with the two PPS-signals by the other DRS4 (DRS4-1), see fig.4. [1] The WR-switch connects via a short 20 m cable to SPEC1, and by 20 m and a 500 m fiber coil to SPEC2. For most measurements, the coil was inside the climate chamber, whereas only for dedicated runs SPEC2 was placed there as well. The DESY climate chamber operates from -20° to +40°.

The data set shown in fig.5 gives the clock jitter of the two WR-SPECs, by measuring the time difference between the PPS pulses coming from both SPECs. The rms of the difference of the two PPS signals (clocks) is <200ps and of same size as the measurment precision of the setup. We emphasize, that no non-statistical fluctuations (eg. short instabilities) have been observed. Thus, the 200 ps (rms) clock stability is stable on a scale of days. We note, that the setup for fig.5 is a somewhat simplified but still very stable WR-master slave configuration: SPEC1 operates as a clock-master (i.e. taking the WR-switch part), directly synchronizing SPEC2 (running as slave).

Figures 6 and 7 show results for one of several 2-day-climate chamber runs, when the temperature cycled between 0° and 30°C, and both 500 m fiber-coil and SPEC2 card were in the chamber. The PPS clock jitter test, shown in fig.6, performs excellent: rms=120 ps, and no non-statistical fluctuations. Figure 7, gives, for the same run conditions, the difference between the recorded trigger times (resolution: 1 ns) from SPEC1 and SPEC2. Both cards trigger the same times, only the neighbouring 1 ns-bins are populated. The 50 ns offset is due to cabeling (10 m).

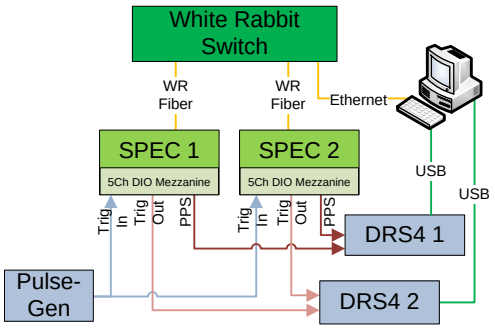

Figure 4: Experimental Setup (baseline configuration). WR fibers are 20 m long to SPEC1 and 520 m to SPEC2. For tests in the environmental chamber, the 500 m WR-fiber and/or the SPEC2 card are located in the DESY-climate chamber.

A large number of additional measuremnts were done, in particular with the fiber-coil exposed to -20° and 30°C. No deviation from the clock stability of <200ps rms as given above were found; also the triggering is absolutely stable and characterized by fig. 7.

4 Conclusion and Outlook

We have shown that the adapted White Rabbit setup, based on a custom made firmware solution, shows excellent performance in a distributed DAQ-system for precision clock-transport, and for time-stamping digital signals with ns-precision. In addition to precision timestamping, the modified WR-node is also capable to generate the trigger on-board, by GHz-sampling an incoming analog signal, and applying smart digital trigger algorithms (running

1. All few-ns offsets between clocks can be traced back to the setup cabeling; since the challenge is perfect stability, these trivial offsets have been ignored.

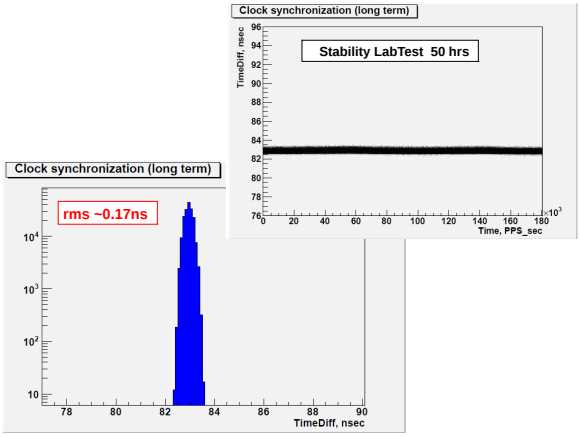

Figure 5: Laboratory-Measurement: Distribution of time difference between PPS-clock-pulses from SPEC1 and SPEC2, for a 50-hours run, see fig. 4 (modified). The right plot shows the time dependence.

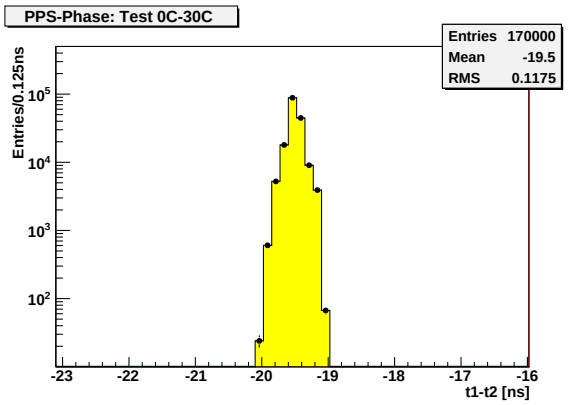

Figure 6: Laboratory-measurement in climate chamber: Distribution of time difference between PPS clock-pulses from two WR-nodes (SPEC1 and SPEC2), synchronized by the WR-master switch, for a 48-hours run. The setup is given in fig. 4. The SPEC2 card and the 500 m fiber-coil were subjected to temperature ramps between 0° and 30^o C.

on the WR-FPGA only). Thus, the White Rabbit unit can turned into a central functional block of a distributed DAQ-system, simplifying precision measurement setups considerably.

Extended tests in an environmental chamber, varying the fiber temperature from -20^{o}C to +40^{o}C and the WR-node from 0^{o}C to +30^{o}C did not yield any significant effect.

The local White-Rabbit clock stability is better than 0.2 ns (rms), and a time-stamping resolution of 1 ns is guaranteed. None of the tests showed any non-statistical instabilities of the clock as well of the time-stamping mechanism; also for relatively abrupt temperature changes.

We note in addition, that besides time-stamping and triggering, the same WR-node can be used for injection of high-precision (ns) test-pulses into any components of a distributed DAQ-system. This opens, for large-scale experiments, unique and unprecedented experimental possibilities for testing and calibration with complicated time-

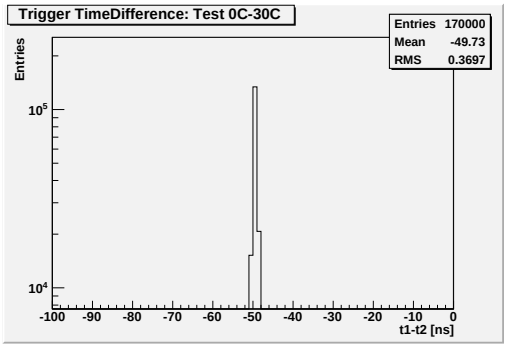

Figure 7: Laboratory-measurement in climate chamber: Distribution of time difference between trigger time stamps from two WR-nodes (SPEC1 and SPEC2), synchronized by the WR-master switch, fed by an instantaneous signal, for a 48-hours run. The setup is given in fig. 4. The SPEC2 card and the 500 m fiber-coil were subjected to temperature ramps between 0° and 30^o C.

patterns from WR-nodes for local units (stations/cameras), as well as to inject ns-coherent test-patterns over the whole array of WR-nodes (a full scale experiment). Firmware development and tests regarding this feature are in preparation.

We conclude, that this White Rabbit system is ready to be applied under field conditions in large-scale astroparticle physics experiments - for time synchronization with nanosecond precision between individual detectors, distributed over km-scale. A first application was the HiSCORE prototype detector in 2012/13 [4], another could be in the near future the CTA-project [10].

Acknowledgment: We acknowledge very helpful discussions, technical advices and support from the White Rabbit community (in particular the CERN based team and A. Rubini) during all phases of this project. The technical support from both SevenSolutions and Creotech was very helpful. We acknowledge the financial support from the Helmholtz association (grant HRJRG-303).

References

[1] Pedro Moreira et al., White Rabbit: Sub-Nanosecond Timing Distribution over Ethernet, ISPCS 2009, `www.iiss.oeaw.ac.at/files/pub/Moreira2009.pdf` J.Serrano et al., The White Rabbit Project, ICALEPCS 2009, `accelconf.web.cern.ch/accelconf/icalepcs2009/papers/tuc004.pdf`
[2] M.Tluczykont, D.Hampf, D.Horns et al., Advances in Space Research 48 (2011) 1935-1941.
[3] R.Wischnewski et al., "Status of the HiSCORE experiment", these proceedings ID-1164
[4] M.Brückner et al., "Results from the WhiteRabbit sub-nsec time synchronization setup at HiSCORE-Tunka", these proceedings ID-1158
[5] M.Tluczykont et al., Nucl. Inst. Meth. A692 (2012) 246.
[6] D.Hampf, D.Horns and M.Tluczykont, Nucl. Instr. Meth. A712 (2013) 137-146
[7] T.Włostowski, Precise time and frequency transfer in a White Rabbit network, Master thesis Warsaw University of Technology, 2010/2011
[8] WR-supplier: SevenSols, Spain, `http://www.sevensols.com`
[9] WR-supplier: Creotech, Poland, `http://www.creotech.pl/en`
[10] K.Bernlöhr et al. (for the CTA-consortium), Astroparticle Physics 43 (2013) 171-188.