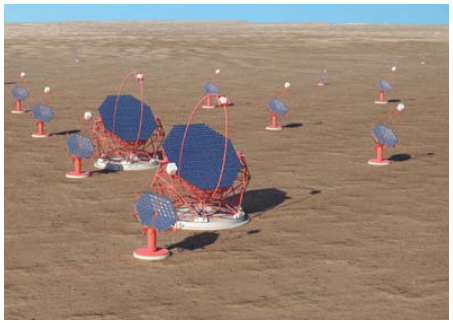
Array Time Synchronization -

First Tests with WhiteRabbit



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CTA-Collaboration Meeting,
Amsterdam,
14.5.2012

HELMHOLTZ ASSOCIATION

DESY

Outline

- Array Time Synchronization for large distributed arrays
  - A generic job, for expt's like CTA, HiSCORE, KM3Net, LHAASO, AUGER-Next, …
  - Can we avoid custom solutions
- WhiteRabbit for Time Synchronization
  - Synchronization & TimeStamping – WRabbit features & architecturs
  - WRabbit is HiSCORE's top candidate; final verification planned for summer 2012
  - CTA would easily fit
- First Tests of WR-performance
  - Results Lab- and field-tests
- Summary

Array Time Synchronization : The Task

- Time Synchronization of large distributed arrays
  - Experiments like HiSCORE (10km2), CTA (few km2), KM3Net, AUGERnext, LHAASO
  - Independent detector units (eg. Cameras, PMT-DAQ-stations, Particle-Detectors)
  - They generate a “local trigger” - this needs to be time-stamped
- Two Tasks:

  (1) **Synchronize clocks in all detector units** to a common central clock with nsec precision;

  Focus: relative timing between detector units must be correct at any moment (not absolute time)

  (2) **Must verify timing precision: long-term monitor / control in-situ**, for at least a subset of the array.

  Verification by an independent system is as important as the synchronization;
  and a comparable in technical challenge
- White Rabbit
  - An excellent candidate
  - In reality: a system (still) under development; verification is needed

White Rabbit

White Rabbit – a new CERN-based extension to Ethernet for :

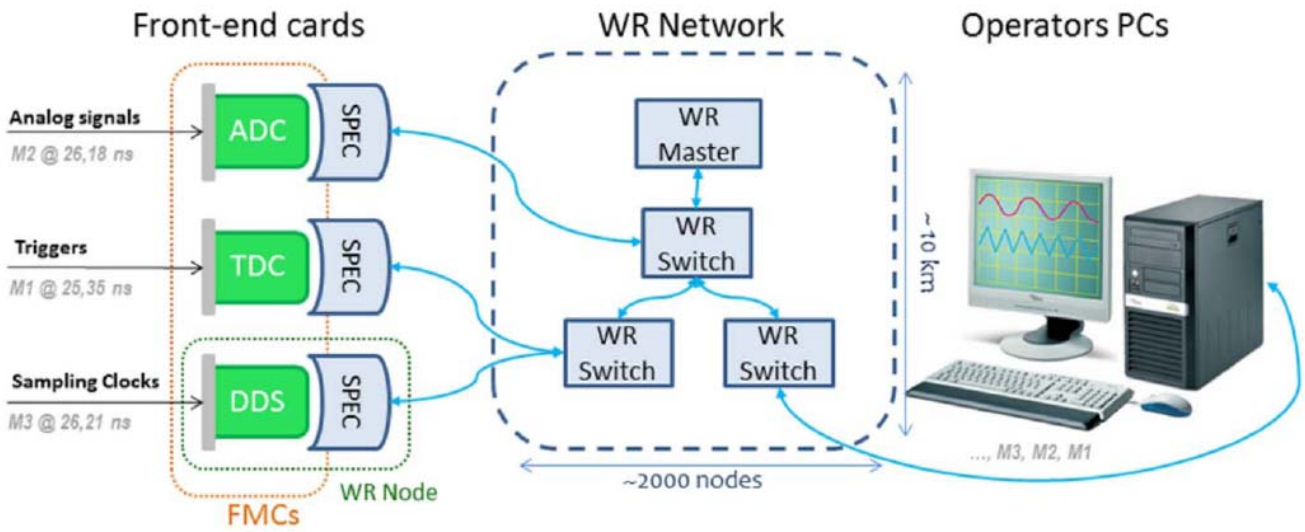
- Synchronous mode (clock synchronization)
- Deterministic routing (package latency guaranteed)

- ~1 ns precision, 20 ps jitter
- 10 km fiber links
- Up to 2000 nodes

- Development for CERN & GSI accelerator complex; much external interest
- Open Hardware Project w/ peer review (ie. open for extensions)
- Hardware is commercially available
- Standardization planned (IEEE…)
- A guaranteed large user community: will be well debugged …

DESY

White Rabbit



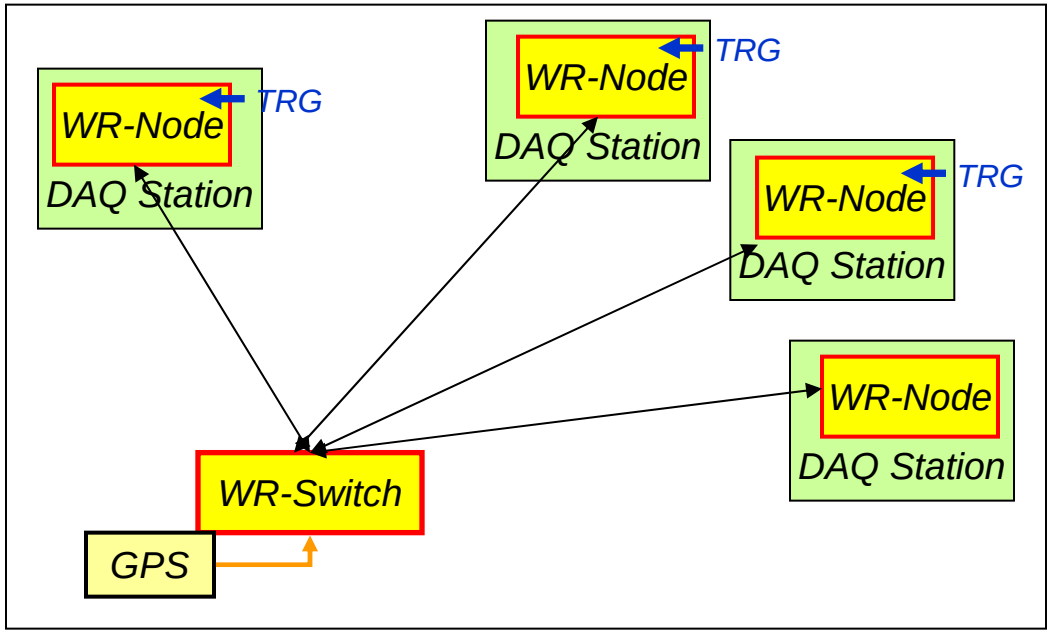
- **For concept + details, see eg:**
  Cern-WR-site http://www.ohwr.org/projects/white-rabbit/wiki ;
  (also http://znwiki3.ifh.de/TUNKA/)

Basic Layout of a WhiteRabbit based timing DAQ

White Rabbit DAQ architecture:

(1) A WR-network
>=1 WRSwitch + GPS/RbCl

(2) Many WR-Nodes ('endpoints')
for time-stamping



Components

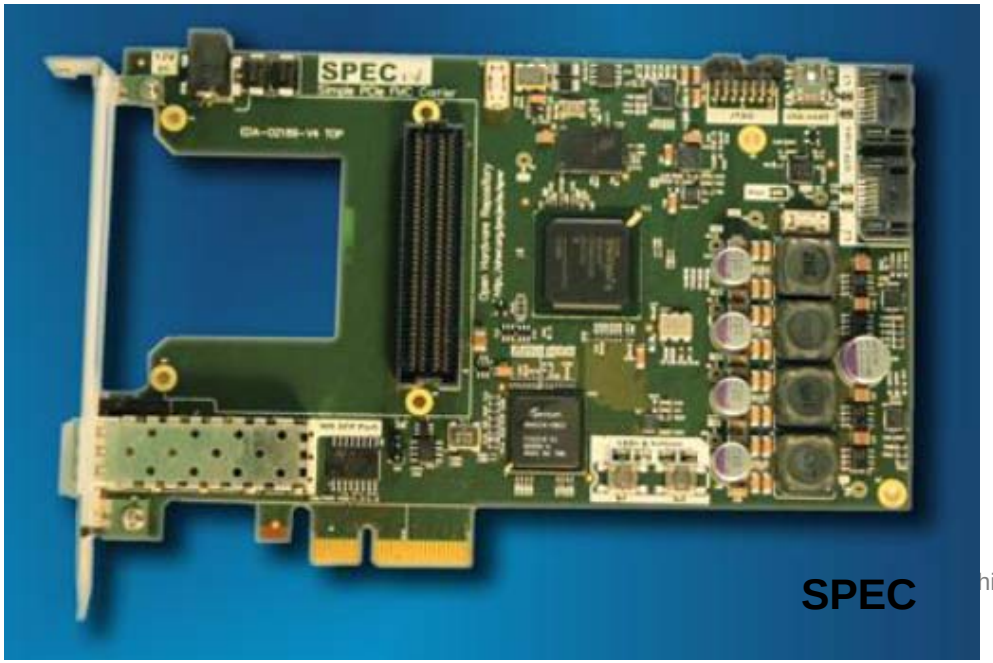
- **WhiteRabbit Switches (WRS)**
- **White-Rabbit Nodes**
  eg. SPEC (*S*imple *P*CI*e* FMC *C*arrier)
  (or build your own board: OWHR)

from June/2012

available

The White-Rabbit SPEC Card

- **SPEC ("Simple PCIe FMC Carrier") is the WR node currently available.**
- **For tests, it can also be configured as WR-Master.**
- **It carries the mezzanine-card for your DAQ:**
  available/planned
  - **Digital InpOutFMC / FMC DEL / FMC FADC(100MHz) / TDC;**
  - **eg. possible: design a DRS4-based mezzanine for HiSCORE/CTA**



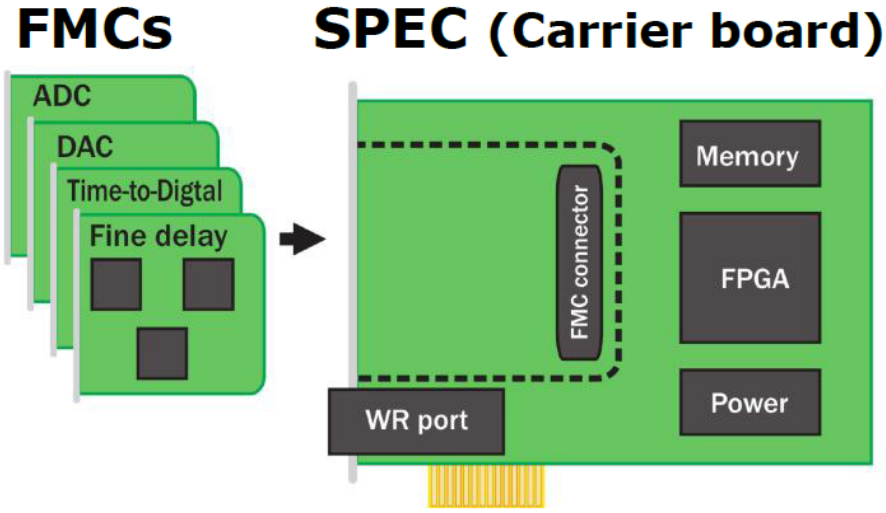
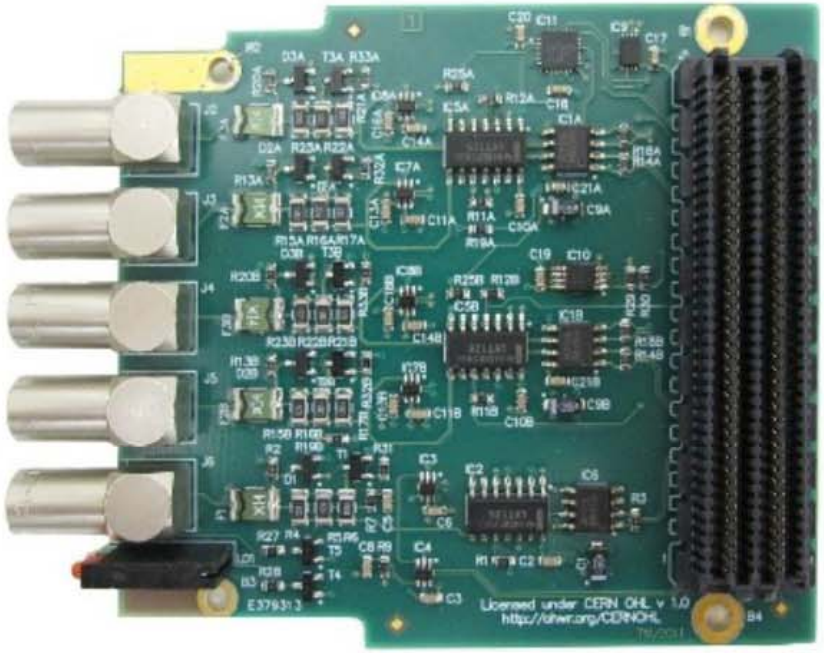


Illustration of the connection of SPEC with FMCs

FMC-DIO-5CHTTLA FMC 5-CHANNEL DIGITAL I/O MODULE

The *fmc-dio-5chttla* 5-channel digital I/O module is a simple board for digital I/O on LEMO connectors.
It has been designed for testing White Rabbit functionality as part of the SPEC Demonstration Package for White Rabbit (**manual**), and it can be used for other applications too.



FUNCTIONAL SPECIFICATIONS

- 5 input/output ports (Lemo 00 connectors)
- Output levels: LVTTL, capable of driving +3.3 V over a 50-Ohm load. At power-up the outputs should be in Hi-Z state
- Input levels: any logic standard from Vih = 1 V to Vih = 5 V (programmable threshold)
- Output Rise/fall times: max. 2 ns
- Input bandwidth: min. 200 MHz
- Programmable 50-Ohm input termination in each channel
- LVDS I/O on the carrier side
- One of the inputs shall be capable of driving a global clock net in the carrier's FPGA
- Inputs need to be protected against +15V pulses with a pulse width of at least 10us @ 50Hz (with protection diodes if possible)
- Withstands a continuous short-circuit on all the outputs at the same time

Example Layout for HiSCORE (CTA)

HiSCORE / EA : 20-40 DAQ-Stations

CTA : 50-100 Telescopes

> Array center:

WR-switches (18 x out) - with N=4 → 67 Stations / Telescopes

(+ central GPS; or Rub.Clock)

> Dedicated SM-fiber to every Station / Telescope

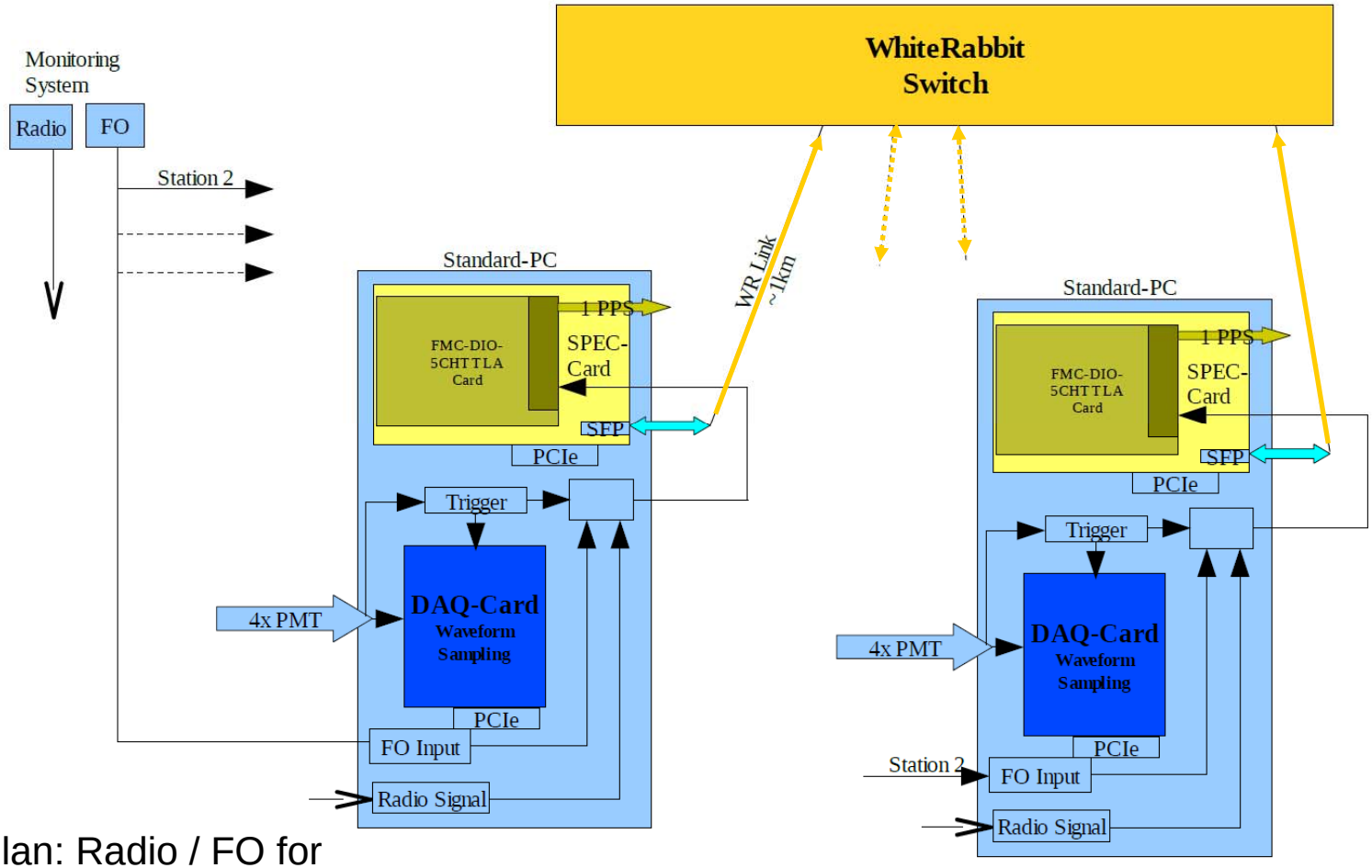
> Every Station / Telescope houses 1 WR-SPEC time-latching unit

> Price: *O(1300Eur) per station*

= 1100 (SPEC+DIO) + 1/17 x 3500 (WRS)

(very conservative)

HiSCORE : DAQ Station + White Rabbit



Resp.: >1 White Rabbit Switches

Plan: Radio / FO for verification of timing

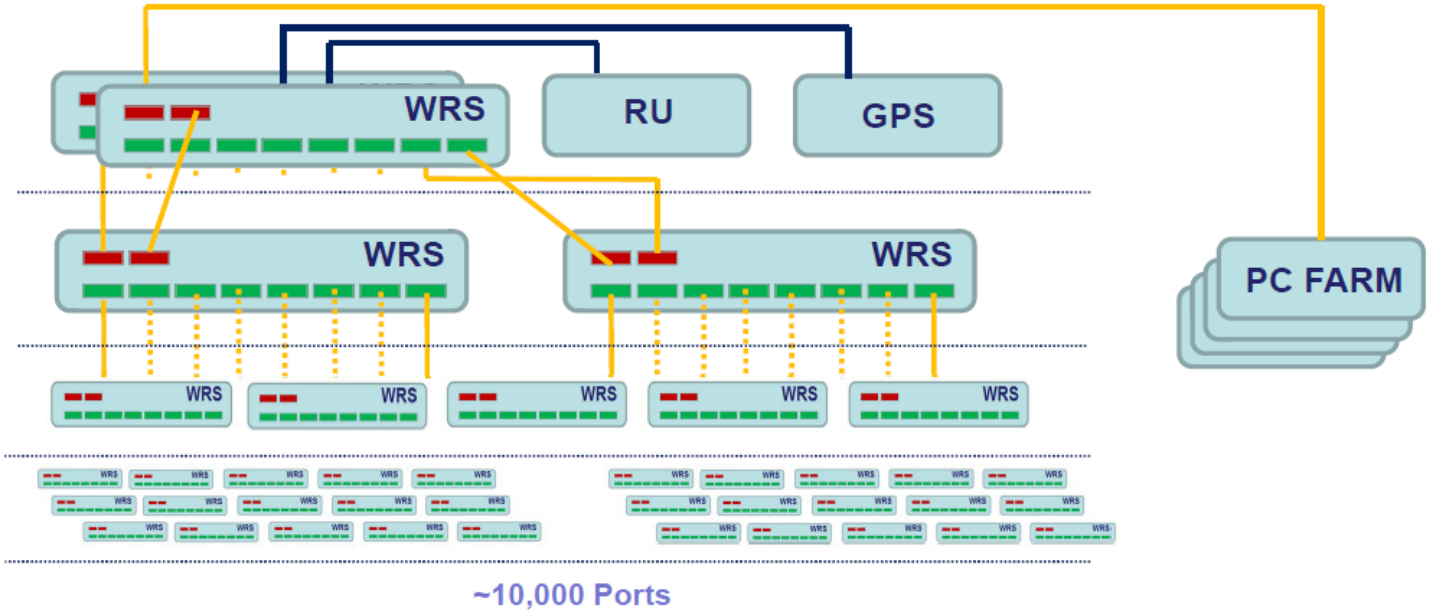
(still under development)

LHAASO : WR plans

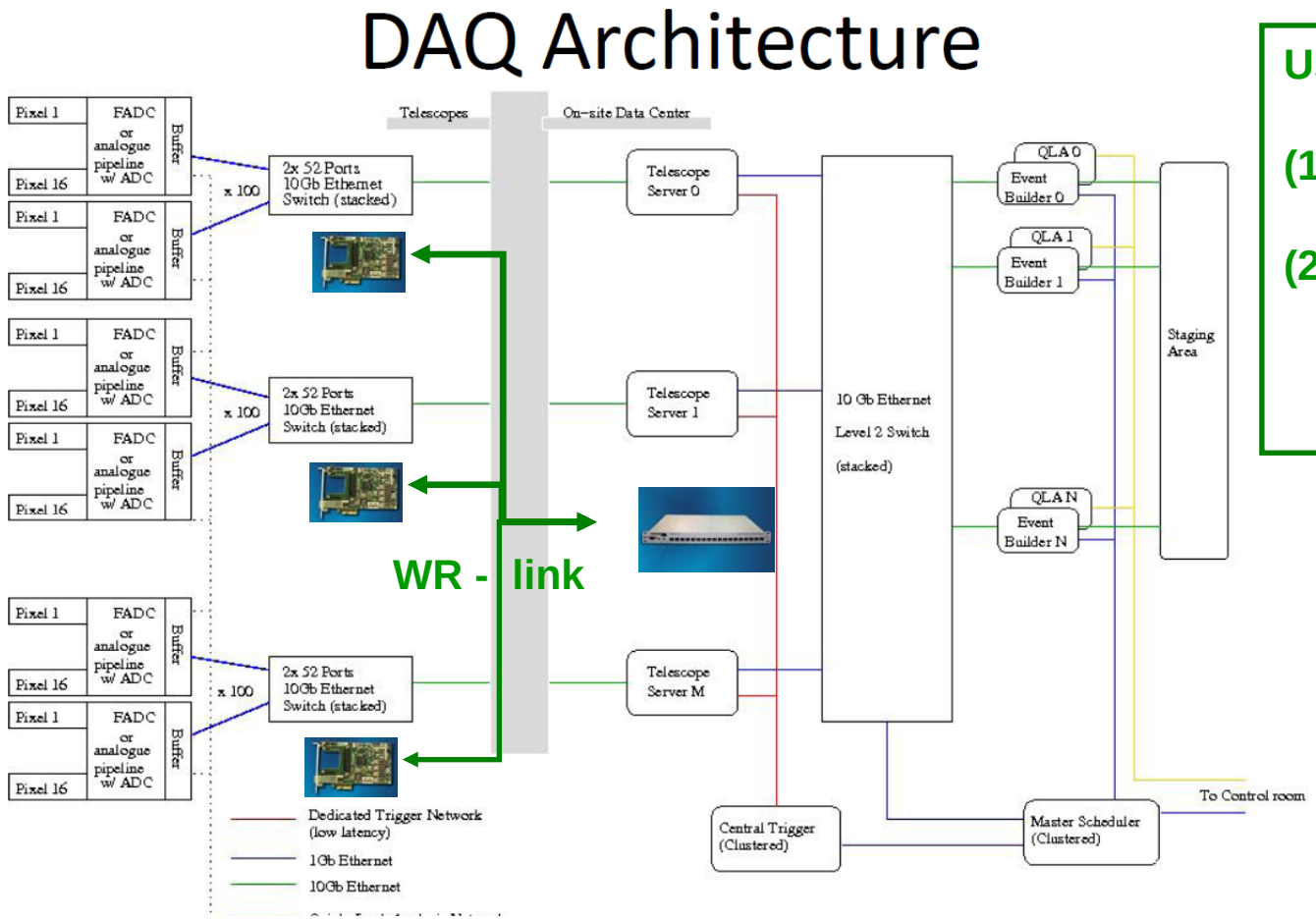
> Other WR-application proposals:

- **LHAASO : ~10000 nodes to synchronize**

Design study
G.Gong, ICALEPCS, 2011.



CTA : DAQ with White Rabbit - Timing & ArrayTrigger



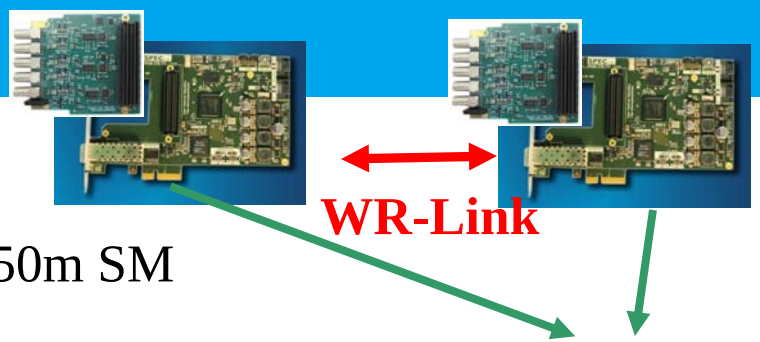
Use the WR-link for

(1) nsec-timing, and

(2) Array-trigger request/ confirm messages (1Gbs) with guaranteed latency.

Here, we considered just the baseline functionality: Time-stamping of Camera trigger.
There many are more options, including development of CTA-WR boards;
Which could integrate FE/DAQ components with WR-cores.
E.g.: a WR-Mezzanine with DRS4 (or NecTar).

Test Setup + Results

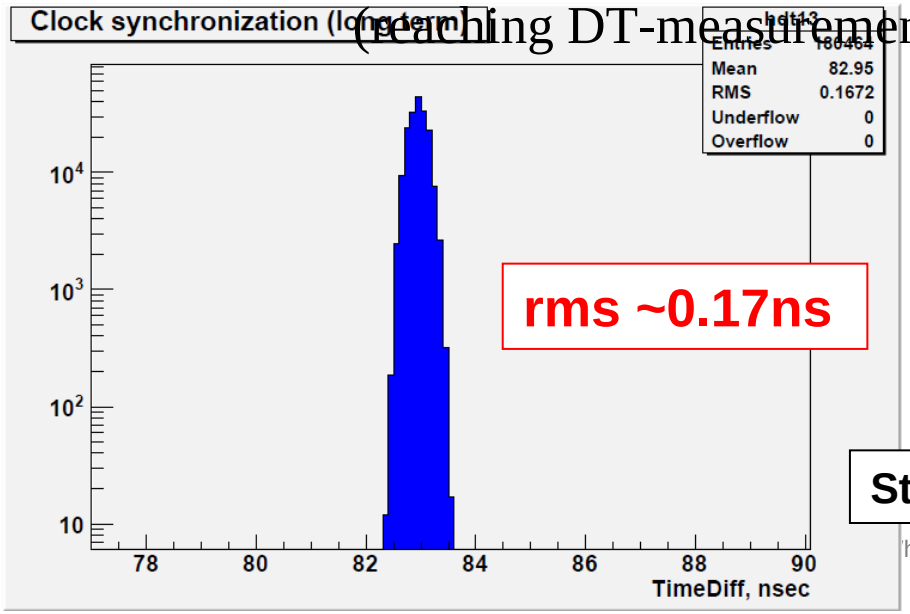


> **Setup:**

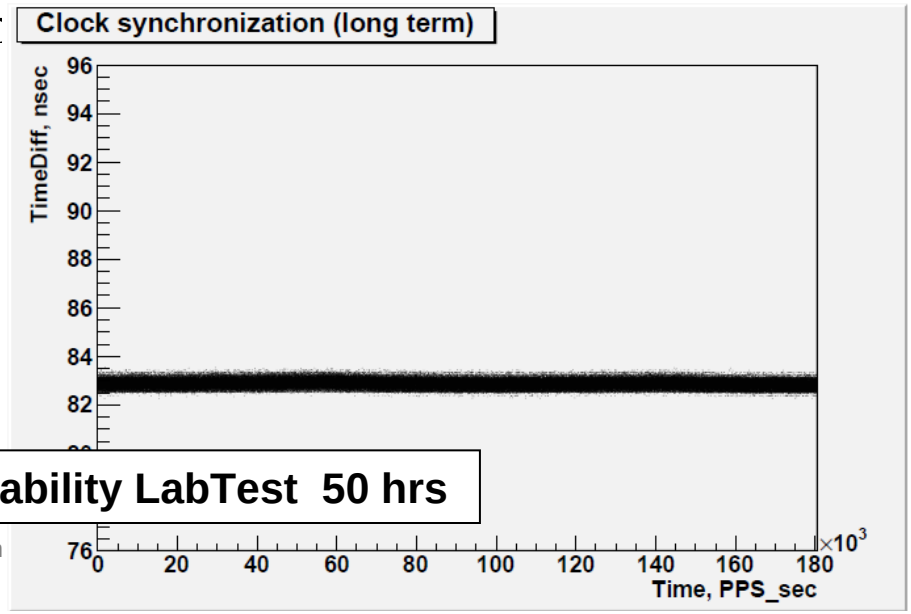
- 2 WR-SPECs: Master-Slave WR-link + 50m SM
- Time tests: comparing the master/slave 1-PPS output
- Setup emulates the basic element: WRS+SPEC

Not sensitive to (1) fluctuations at <<1sec scale, and (2) clocks in neighbouring nodes

> **Result:** **TimeDiff (Master-Slave) rms < 0.2 ns !!**



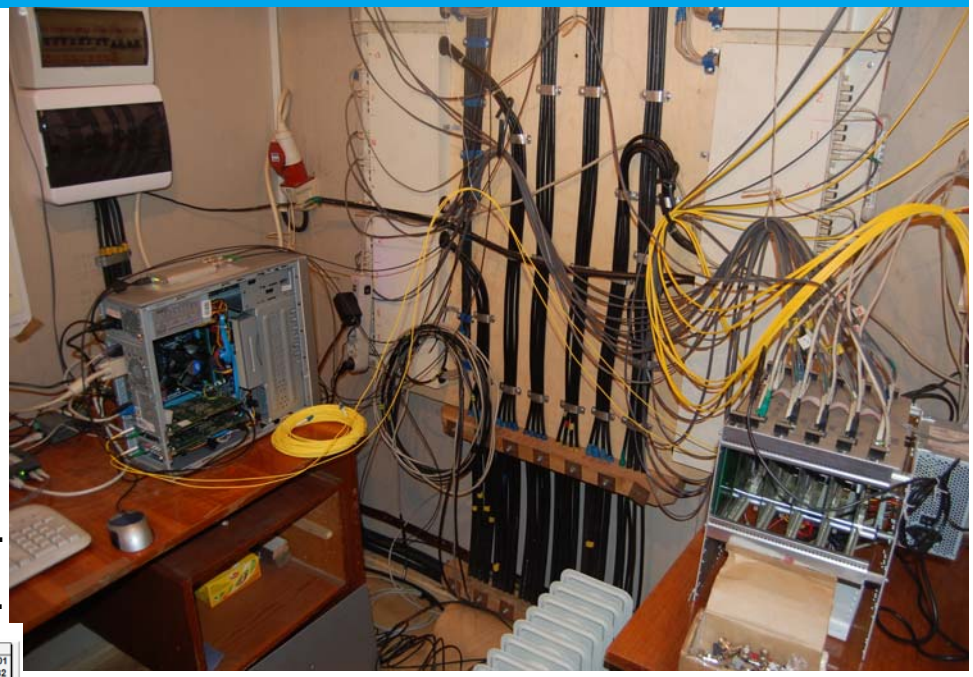
(reaching DT-measurement)

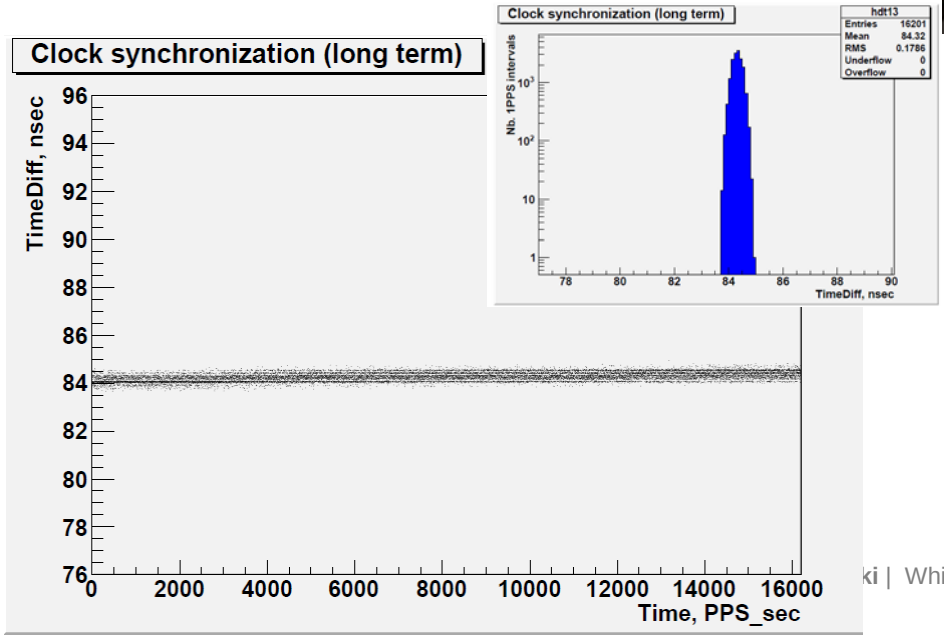


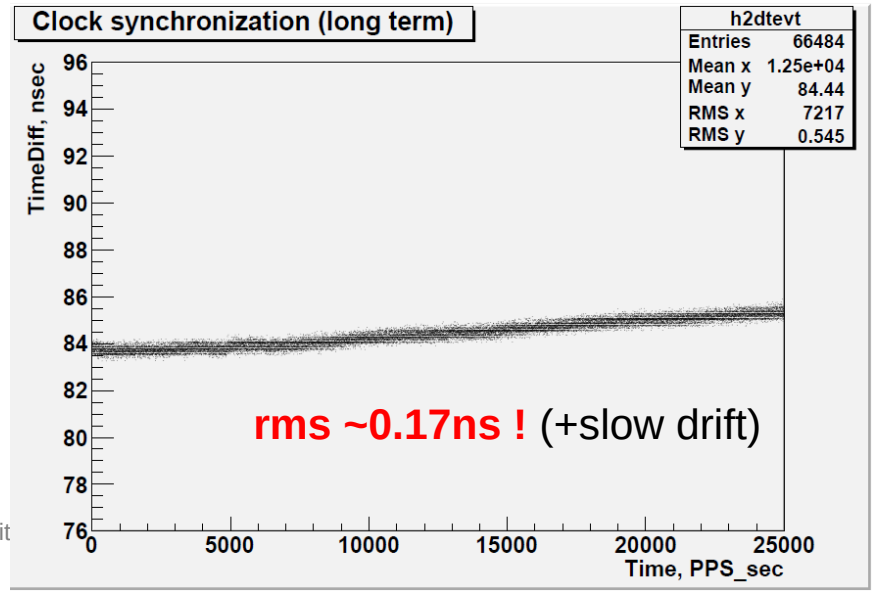
Test at Tunka/HiSCORE

- Field tests at Tunka/HiSCORE site
  - April 2012: use DESY-Lab-setup
  - use the real 1+1 km Tunka-fibers
- Confirmed Lab-result: rms <0.2 ns
  - Routine operation/tests in summer 2012; slow drifts (temperature?),external noise.

  Like any in-situ verification of a new system.







Summary

- First Tests of basic White Rabbit elements are very encouraging:
  - <0.2ns longterm stability is possible.
  - Next step: realistic setup WRS + 2-3 nodes
- White Rabbit is a realistic candidate as time-synchronization system in new APP projects.
  - WR: will be the HiSCORE / EA timing system
  - HiSCORE prototype, starting Oct.2012, can serve as reference system
  - Applications in current experiments is realistic and would be helpful (eg. backup-timing)
- Advantages, that make WR a top candidate for CTA:
  - A real standard, commercial support, synergies with other users (!)
  - Opens source, adaptable to specific needs
  - Reliability, easy maintenance, cost effective, scalability, field-applicable
- With it's commitment to HiSCORE WR-DAQ, DESY is currently investigating a related CTA initiative. Any collaborators: very welcome !!

> Thanks.