

# Phillips Scientific

## 16 Channel Peak ADC

### CAMAC MODEL 7164 7164H

### FEATURES

- \* The Model 7164 has LEMO Inputs
- \* The Model 7164H has Differential Header Inputs
- \* Less Than 7.2  $\mu$ Sec Conversion and Processing Time
- \* 12-Bit Dynamic Range, Resolution to 1 mV/Count
- \* Accepts Unipolar and Bipolar Input Pulse Shapes
- \* Programmable Pedestal Correction
- \* Sparse Data Scan with Lower and Upper Threshold Cuts
- \* Fast CLEAR and Common GATE Window
- \* Built-in Test Features Check ADC and Digitization

### DESCRIPTION

The Model 7164 PEAK ADC implements 16 channels of Peak Detect and Hold followed by a digital processing section and CAMAC interface in a single width CAMAC module. To minimize data readout time, the ADC performs a sparse data function. Channels can be individually programmed with pedestal correction and both lower and upper level thresholds. Digitization starts following release of the Common GATE input. It may be delayed by a user-programmable amount to allow time for derivation of fast CLEAR signals before digitization starts.

Channels that meet the sparsification requirements will have corresponding bits set in the Hit Register. Subsequent events will be ignored until the Hit Register is cleared either by completing a sparse read of the module or via front panel fast CLEAR or CAMAC Clear commands.

### ANALOG INPUTS

Unless otherwise noted, specifications are for single-ended 4.096 Volts full scale and 50 ohm input impedance. Consult factory for available optional ranges up to  $\pm 10V$  full scale and input impedance up to 1K ohm.

**Voltage Compliance** :  $\pm 20mV$  to  $\pm 4.096$  Volts; Either positive, negative or true differential; (Specify when ordering).

**Signal Shape** : Any typical pulse shapes encountered in nuclear physics: Unipolar, Bipolar or Tripolar. Risetimes within the range of 50nSec to 50 $\mu$ Sec.

#### Input Impedance

**Single Ended** : 51 ohm  $\pm 2\%$ , direct coupled.  
**Differential** : 102 ohm  $\pm 2\%$ , direct coupled.

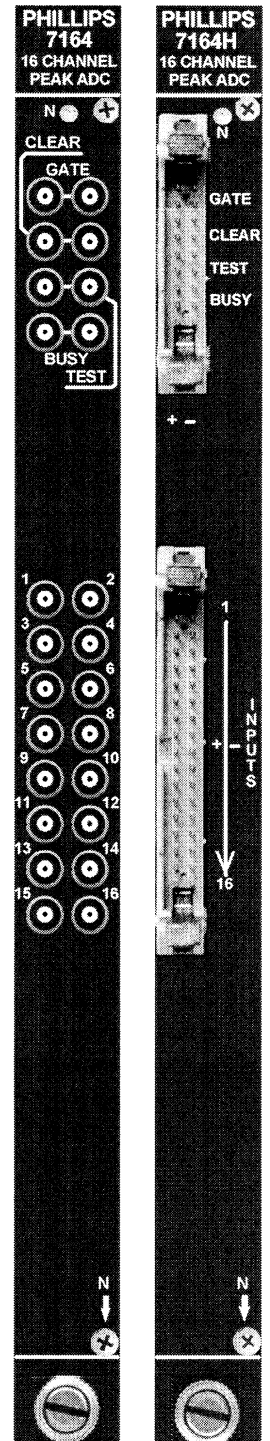
**Dynamic Range** : 4.096V full scale, 1mV/Count.  $\pm 2\%$ , 12-bit Range.

**Input Offset** : 0 to 2mV, (40 $\mu$ Amp) maximum; (20 $\mu$ Amp Differential).

**Slew Rate** : 80Volt/ $\mu$ Sec.

**Stability Gain & Pedestal** : Better than 100 $\mu$ V/  $^{\circ}C$  between 0  $^{\circ}C$  to 60  $^{\circ}C$ .

**Droop** : Less than 50 $\mu$ V/ $\mu$ Sec.



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## **CLEAR, GATE and TEST INPUTS**

- LEMO Inputs (7164)** : NIM logic levels; 2 connectors per input to facilitate daisy chaining. Input impedance 5.1K ohm; 50 ohm terminate the last module in chain.
- ECL Inputs (7164H)** : Differential ECL logic levels; 2 pairs per input to facilitate daisy chaining; terminate at end of chain with 110 ohm.
- Common GATE Input** : Common to all channels; 50nSec to 50µSec; should precede the voltage peak by 20nSec minimum; no dependence on position of analog event within gate. Processing of events begins at end of GATE pulse.
- CLEAR Input** : Common to all channels, accepts 10nSec or greater input width.
- Clear Settling Time** : Less than 850nSec to within one count.
- Clear Function** : Timing assumes no conversion delay, causing digitization to start typically 600nSec after trailing edge of GATE.  
**(End of Gate – 700nSec) < t<sub>CLR</sub> < Start of digitization:** Resets front ends, aborts digitization cycle.  
**t<sub>CLR</sub> > Start of digitization:** No effect on front ends or digitization.
- TEST Input** : Leading edge causes a GATE and analog input to be applied to all channels. Digitizes to approximately 1/4 full scale calibration. NOT intended for precise calibration of the module.

## **BUSY Output**

- LEMO (7164)** : Two paralleled LEMO connectors; Double-amplitude negative NIM logic 32mA.
- ECL (7164H)** : Two pairs of double row pins; Differential ECL logic levels.

Active from the trailing edge of common GATE until the Hit Register has been cleared, explicitly by either the front panel CLEAR input or by one of the CAMAC clear commands, or implicitly by completion of a sparse read function. The CLEAR input signal causes BUSY to go active for 750nSec. The module will not recognize a new GATE while BUSY is active.

## **FRONT END PERFORMANCE**

### **Linearity**

- Integral** : Less than 3 counts over 10% to 90% of range.  
: Dithering disabled: Less than ±0.5LSB from 0 to 4095 counts.
- Differential** : 6-bit dithering: Less than ±0.06LSB from 64 to 4031 counts.  
: 7-bit dithering: Less than ±0.025LSB from 128 to 3967 counts.

**Crosstalk** : 1 LSB maximum between adjacent channels operated within range.

**Conversion Time** : 7.2 µSec maximum; No conversion delay inserted.

**Conversion Delay** : Digitization begins 600nSec after trailing edge of GATE to allow time for settling and for accepting fast CLEAR signals. Digitization may be delayed by 0 to 16µSec in 62.5nSec increments with external jumpers. The increased delay may be used to allow a greater acceptance window for CLEAR signals.

### **Power Supply Requirements :**

- + 6V @ 2.4 Amp typically
  - 6V @ 1.8 Amp typically
  - +24V @ 510 mA typically
- Forced air cooling is recommended.

## ADDITIONAL TEST FEATURES

- Calibration Check** : Simulates a Voltage/Gate sequence under CAMAC control to verify operation of the module. CAMAC selectable nominal 1/20 or 1/4 full scale calibration. Not intended for precise calibration of the module.
- CAMAC Check** : Loads a predetermined pattern to simulate the outputs of the A/D converters. Useful for verifying the operation of the processing sections of the module.

## SPARSIFICATION and LAM OPERATION

Separate pedestals and upper and lower thresholds may be set for each channel. They are enabled using bits in the Control Register. Pedestals in signed 2's complement format are added to the data before threshold comparison. Bits in the Hit Register are set during digitization for those channels whose pedestal corrected data falls within their upper and lower thresholds. If enabled, LAM is set whenever a bit in the Hit Register is set. Sparse data reads present only those channels with bits set in the Hit Register, starting with the highest numbered channel. As channels are read, their Hit Register bits are reset. When the final channel has been read LAM is reset.

## DATA WORD FORMAT

16	13	12	1
Channel ID		Channel Data	

## CONTROL REGISTER FORMAT

16	9	8	4	3	2	1
Conversion Delay (Read Only)	0	UT Enable	LT Enable	PED Enable		

## CAMAC DATAWAY OPERATIONS

- F(0)·A(X)** : Read event data memory for Channel (X+1). Data word as described above.
- F(1)·A(X)** : Read the parameter memory pointed to by the most recent F17 operation for channel (X+1).
- F(4)·A(0)** : Read Sparse Data. Only those channels with data that falls between the upper and lower thresholds are read, starting with the highest numbered channel. Reading an empty buffer returns Q false. Data word as described above.
- F(6)·A(0)** : Read the Control Register. Format described above.
- F(6)·A(1)** : Read the Hit Register. Shows which channels' pedestal corrected data falls within their upper and lower thresholds.
- F(8)** : Test LAM. A Q=1 response is generated if LAM is present and enabled. The address lines have no effect on this command.
- F(9)** : Clear the Module. Resets front end, clears and disables LAM, disables pedestals and thresholds. The address lines have no effect on this command.
- F(10)** : Clear LAM. Occurs on S2 strobe. The address lines have no effect on this command.
- F(11)·A(0)** : Reset the Control Register. Occurs on S2 strobe.
- F(11)·A(1)** : Reset the Hit Register and LAM. No effect on data memory. Occurs on S2 strobe.

## **CAMAC DATAWAY COMMANDS** (continued)

- F(11)·A(2)** : Reset the Test Register. Occurs on S2 strobe.
- F(11)·A(3)** : Reset the Hit Register, LAM and data memory. Occurs on S2 strobe.
- F(16)·A(X)** : Write to data memory for channel (X+1).
- F(17)·A(0)** : Select the Pedestal Memory for the next F1 or F20 operation.
- F(17)·A(1)** : Select the Lower Threshold Memory for the next F1 or F20 operation.
- F(17)·A(2)** : Select the Upper Threshold Memory for the next F1 or F20 operation.
- F(17)·A(4)** : Select the Test Register for the next F20 operation.
- F(19)·A(0)** : Set the Control Register bits. Format described above.
- F(20)·A(X)** : Write the pedestal, upper or lower threshold for Channel (X+1) as selected by the most recent F17 operation. Pedestal range is  $\pm 4095$ ; threshold ranges are 0 to 4095. Program the Test Register if it was selected by the most recent F17 operation.
- A0** : Test pattern = 001001001001  
**A1** : Test pattern = 010010010010  
**A2** : Test pattern = 100100100100  
**A3** : Test pattern = 111111111111
- F(23)·A(0)** : Reset the Control Register bits. Format described above.
- F(24)** : Disable LAM. Occurs on the S2 strobe. The address lines have no effect on this command.
- F(25)·A0** : Digital test. Initiates a data acquisition cycle using the value stored in the Test Register by the most recent F20 command.
- F(25)·A1** : Test. Initiates a data acquisition cycle using a simulated event of approximately 1/20 full scale applied to the front end.
- F(25)·A2** : Test. Runs a data acquisition cycle using a simulated event of approximately 1/4 full scale applied to the front end.
- F(26)** : Enable LAM. Enables LAM on the S1 strobe. The address lines have no effect on this command.
- C, Z** : Reset the front end, clear and disable the LAM, disable pedestal and thresholds and clear the Hit Register. Occurs on the S2 strobe.
- I** : Inhibits peak detector front end.