VMDIS 8004

VME / VSB display & diagnostic module

Getting Started Manual, version 1.0

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CREATIVE ELECTRONIC SYSTEMS S.A.

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1. GENERAL INFORMATION

1.1 Description

The VMDIS 8004 is a brand-new VME / VSB Display and Diagnostic Module, essential to monitor the backplane activity of modern VME / VSB systems and measure the performance of VME transfers.

The VMDIS 8004 is an extension and an improvement of the VMDIS 8003, providing additional visual and computer controlled test features.

- It has been designed to monitor modern VME systems using D64 and / or the VSB bus. The display can be switched from VME to VSB by a front-panel switch.
- Another function of the card is to provide extended VME test features when booting a VME based microprocessor system. All data, address and control lines of the VME and VSB busses are latched in a set of registers which can be read from the VME bus.
- The VMDIS 8004 provides an interrupt input which is routed to VME. This feature is extremely useful when debugging software requiring interrupt handling. The interrupt input can be manually controlled, software controlled or controlled by a remote instrument driving a TTL / NIM LEMO input on the front-panel.
- The VMDIS 8004 is also able to count the number of data transfers during VME or VSB block transfers. This feature is of great help when debugging DMA transfers. It is also equipped with timing logic which measures the duration of VME / VSB cycles.
- Finally, the VMDIS 8004 can be configured as high speed VME slot 1, supporting all the VME arbitration schemes. When the module is plugged in VSB slot 0, it can be enabled to be VSB Central Arbiter.

Block Diagram

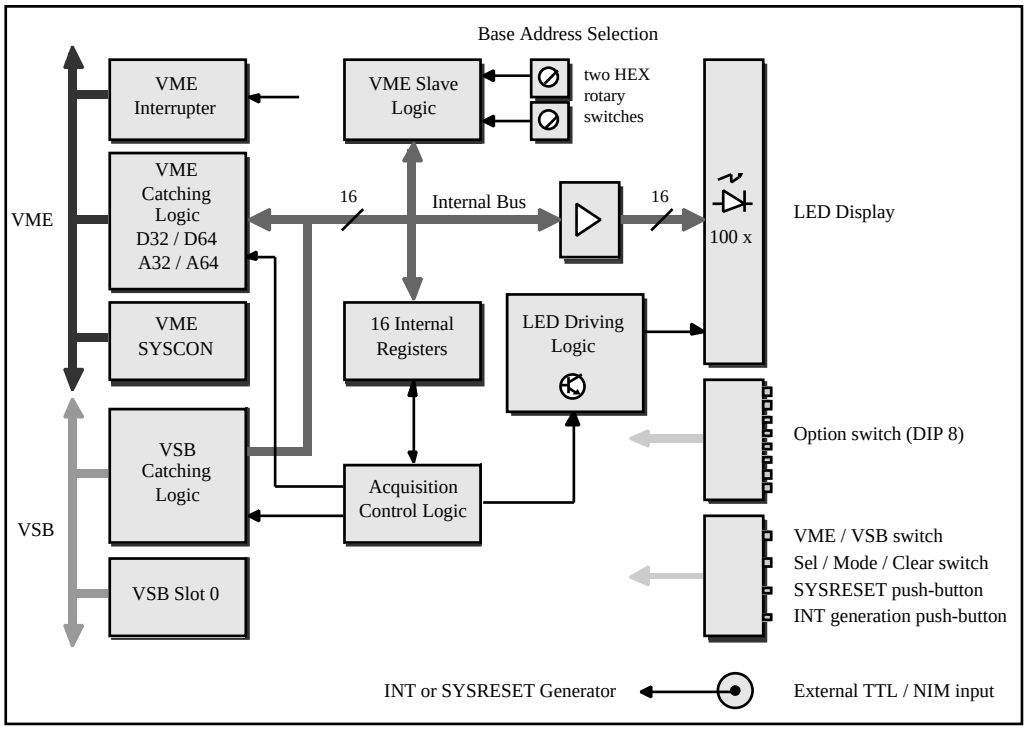

Fig 1.1

1.2 Features

VME LEDs display	• LEDs display of all VME signals:
	  • Address Lines, including A64
	  • Data Lines, including D64
	  • Address Modifier Lines
	  • Control Lines
	• Transparent static mode
	• Latched mode
	• Monitor mode, responding to AM = $14

VME high-speed slot 1	• VME central arbiter PRI / RRS • VME arbitration time-out • VME BTO logic with value 15 µs or 255 µs • VME 16 MHz SYSCLK generator • IACK daisy-chain driver • Power-up SYSRESET
VME interrupter	• VME interrupter, activated by front-panel push-button or external signal (NIM / TTL) or LEMO 00 • VME interrupt can be generated in response to software request • Level selectable by jumper. • Status / ID select by jumper.
VME SYSRESET	• VME SYSRESET, activated by front-panel push-button or external signal (NIM / TTL) or LEMO 00 • VME SYSRESET can be generated in response to software request • Minimum pulse calibrated according to VME specs.
VME Read-back	• Control and Status registers accessible over VME through a VME Slave interface • 256 bytes mapped in A16. • Base address selectable by rotary switches • Read back of all catching registers
Special Purpose	• Block transfer counter and Cycle duration timer • Delay between DS and DTACK programmable in monitoring mode
VSB LEDs display	• LEDs display of all VSB signals. • Transparent static mode. • Latched mode.
VSB slot 0	• VSB central arbiter (enabled if slot 0 with jumper).

1.3 VME / VSB Mode Selection

The VMDIS LED's display can be selected for VME or VSB through the front panel switch.

on right (VME) displays the VME signals.
on left (VSB) displays the VSB signals.

The reader can find in the following table the correspondence between VME and VSB mode for each LED of the front panel according to the mode selected.

	VME mode	***VSB mode***
Dxx	D32 VME Dxx signal D64 VME Dxx signal in data phase A64 VME Dxx signal in address phase	VSB ADxx signal in data phase
A00	D32 Not used D64 VME LWord* signal in data phase A64 Not used	VSB AD00 signal in address phase
Axx	D32 VME Axx signal D64 VME Axx signal in data phase A64 VME Axx signal in address phase	VSB ADxx signal in address phase
AM0 (SPC0)	VME AM0 signal	VSB SPACE0 signal
AM1 (SPC1)	VME AM1 signal	VSB SPACE1 signal
AM2 (SIZ0)	VME AM2 signal	VSB SIZ0 signal
AM3 (SIZ1)	VME AM3 signal	VSB SIZ1 signal
AM4 (ASK0)	VME AM4 signal	VSB ASACK0* signal
AM5 (ASK1)	VME AM5 signal	VSB ASACK1* signal
LWD (LOCK)	D32 VME LWord* signal (ON: LWord* is active) D64 VME LWord* signal A64 VME LWord* signal	VSB LOCK* signal. (ON: LOCK* is active)
AS (PAS)	VME cycle detected (stretched)	VSB cycle detected (stretched)
DS0 (DS)	VME DS0* signal	VSB DS* signal
DS1	VME DS1* signal	Not used
WR (WR)	VME Write* signal. (ON: Write cycle)	VSB Write* signal. (ON: Write cycle)
DTAC (ACK)	VME DTACK* signal	VSB ACK* signal
BERR (ERR)	VME BERR* signal	VSB ERR* signal
RETY (CACH)	VME RETRY* signal	VSB CACHE* signal
LBTO (ADER)	Local BTO generated	Address error detected
ACF	VME ACFAIL* signal (stretched)	VME ACFAIL* signal (stretched)
SYSF	VME SYSFAIL* signal (stretched)	VME SYSFAIL* signal (stretched)
SCLK	VME SYSCLK signal	VME SYSCLK signal
SRES	VME SYSRESET* signal (stretched)	VME SYSRESET* signal (stretched)
INTP (INTP)	Local Interrupt Pending	Local Interrupt Pending
BR0 (BREQ)	VME BREQ0* signal (stretched)	VSB BREQ* signal (stretched)
BR1	VME BREQ1* signal (stretched)	Not used
BR2	VME BREQ2* signal (stretched)	Not used
BR3	VME BREQ3* signal (stretched)	Not used
BBSY	VME BBSY* signal	VSB BSY signal

	VME mode	*VSB mode*
IACK	VME IACK* signal	Not used
IRQ1 (IRQ)	VME IRQ1* signal	VSB IRQ* signal
IRQ2	VME IRQ2* signal	Not used
IRQ3	VME IRQ3* signal	Not used
IRQ4	VME IRQ4* signal	Not used
IRQ5 (GA0)	VME IRQ5* signal	VSB GA0 signal
IRQ6 (GA1)	VME IRQ6* signal	Not GA1 signal
IRQ7 (GA2)	VME IRQ7* signal	Not GA2 signal
AC (AC)	Not used	VSB AC signal
WAIT (WAIT)	Not used	VSB WAIT* signal (stretched)
STOP (STOP)	VMDIS 8004 is in STOP state	VMDIS 8004 is in STOP state
DIR (DIR)	VMDIS 8004 is in VME DIRect mode	VMDIS 8004 is in VSB DIRect mode
LAT (LAT)	VMDIS 8004 is in VME LATched mode	VMDIS 8004 is in VSB LATched mode
MON	VMDIS 8004 is in VME MONitor mode	Mode not implemented in VSB mode
VMEC (VMEC)	VMDIS 8004 is VME system controller	VMDIS 8004 is VME system controller
VSBC (VSBC)	VMDIS 8004 is VSB slot 0	VMDIS 8004 is VSB slot 0

Please refer to § 5.1 for a visual location of those LEDs.

More information about the "stretched" signals can be found in § 2.3.

1.4 Display Mode of Operation

The VMDIS 8004 can be set in 3 modes of operation which are:

Direct Mode

The LEDs reflect the real state of the concerned VME or VSB signals with **no** logical intervention. The LED is ON when the signal is active (take care that active low signals will light the corresponding LED when they are in a low level).

In this mode, it is possible to check that no VME line is driven permanently by another module.

Latched Mode

In this mode, every VME transaction is displayed on the front panel.

The LEDs reflect the state of a catching flip-flop or a stretching monostable. The concerned VME or VSB signal is latched at every cycle and remains in its memorised state until a new cycle is captured, or is stretched with a 350 ms pulse and read back in the VMDIS registers for examination.

Monitor

In this mode, the VMDIS 8004 does not display and memorises every transaction occurring on the VME backplane, but only those matching an AM code = $14.

The purpose of this mode is to perform a computer-controlled test for large VME systems by writing data into the VMDIS from a CPU and reading them back (VMEDATL & VMEDATH registers, A16 mode) to check for discrepancies.

Mode of Operation Selection

The VMDIS mode of operation can be selected either from the CSR space (CSR0 Register, refer to § 4.2) or through the front panel push-button "SEL" (SW2, refer to § 5.2 for location).

An action at right (SEL) on the front panel SW2 push button changes the mode of operation according to the step by step state machine described in figure 1.2 for the VME mode and figure 1.3 for the VSB mode.

VME Mode Selection State Diagram

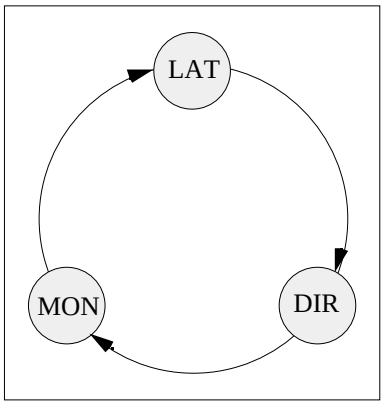

Fig 1.2

VSB Mode Selection State Diagram

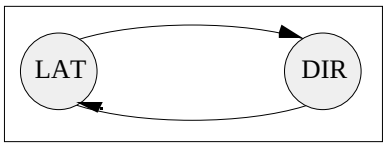

Fig 1.3

The mode of operation is reported on the front panel LEDs as:	
LAT	Latched, cycle memorised on each VME or VSB event.
DIR	Direct, display reports steady state of the respective bus signals.
MON	Monitor, cycle memorised only with the selected AM code for monitor.

1.5 Clearing the Display

The Clear function is also implemented with SW2 (refer to § 5.2). When this switch is pressed at left (CLR), all LEDs of the display are cleared until a new VME / VSB cycle is detected (depending upon the position of the VME / VSB switch). Of course, the Clear function is meaningful only when the VMDIS 8004 is in latched mode.

The Clear is also used to reset the Trigger logic when the VMDIS is in STOP state.

1.6 Trigger Function

To facilitate the tracking of VME or VSB events, the VMDIS 8004 can be forced in a STOP state, latching the VME / VSB current cycle, under one of the following conditions:

VME

Event	Switch	The VMDIS 8004 goes in STOP after
Stop on IACK cycle	DSW3 ON	it detects a VME interrupt acknowledge cycle
Stop on ERROR	DSW4 ON	it detects a VME cycle acknowledged by a BERR*

VSB

Event	Switch	The VMDIS 8004 goes in STOP after
Stop on IACK cycle	DSW3 ON	it detects a VSB interrupt acknowledge cycle (SPACE 1, 0 = 00)
Stop on ERROR	DSW4 ON	it detects a VSB cycle acknowledged by a ERR* or when AC is going high with ASACK* 1, 0 = 00

This last condition (AC going high with ASACK* 1, 0 = 00) is also an error because it means that no VSB slave device is responding to the cycle.

While the VMDIS 8004 is in STOP mode the LED "STOP" is ON.

When the VMDIS is in STOP state, it will stop acquiring cycles and the user can look at the front panel LED display the last cycle captured. To clear the STOP case (going back in normal mode) the user should press the Clear switch once (SW2).

2. VME DISPLAY MODE

2.1 VME Cycle Memorisation

The VME cycles signals are temporary memorised in registers with strobes related to the VME cycle. The VME cycles are caught whatever the VMDIS 8004 is in VSB or VME mode.

❶ When the VMDIS 8004 is in DIRect mode, the catching register are set in transparent and every cycle is displayed.

❷ When the VMDIS 8004 is in LATched mode, every VME cycle not decoded to access to internal VMDIS 8004 registers or every VME IACK cycle (even if the VMDIS 8004 is interrupter) is caught and displayed.

❸ When the VMDIS 8004 is in MONitor mode, every cycle with an AM code equal to $14 is memorised and displayed.

2.2 Data and Address Bus Display Selection

Data and Address Bus Sizes

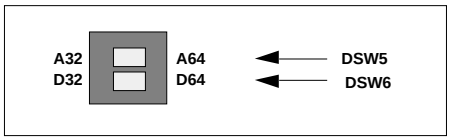

Fig 2.1

You have 2 possibilities to control the data and address bus displaying:

By the DIP Switch positions DSW5 and DSW6, as shown on fig. 2.1.

By writing in the CSR0 register (refer § 4.2), bits <05...04>. In this case, you must let the front panel DIP Switches DSW5 & DSW6 in positions A32 & D32.

According to these different options, the VMDIS 8004 can be used to display:

❶ The 32 Address lines and the 32 Data lines in option A32 / D32. In this case:

- the "D00...D31" LEDs display the <D00...D31> physical data lines of the VME cycle
- the "A00" LED is insignificant and always OFF
- the "A01...A31" LEDs display the <A01...A31> physical address lines of the VME cycle

❷ The 64 Address information in option A64 / D32 or A64 / D64. In this case:

- the "D00...D31" LEDs display the <D00...D31> physical lines of the VME cycle during the address phase and which contain the <A32...A63> address information
- the "A00" LED is insignificant and always OFF
- the "A01...A31" LEDs display the <A01...A31> physical lines of the VME cycle during the address phase and which contain the <A01...A31> address information

❸ The 64 Data information in option A32 / D64. In this case:

- the "D00...D31" LEDs display the <D00...D31> physical lines of the VME cycle during the data phase and which contain the <D00...D31> data information
- the "A00...A31" LEDs display the LWORD* and <A01...A31> physical lines of the VME cycle during the data phase and which contain the <D31...D63> data information

Correspondence between what is on the bus and what is displayed during a write access

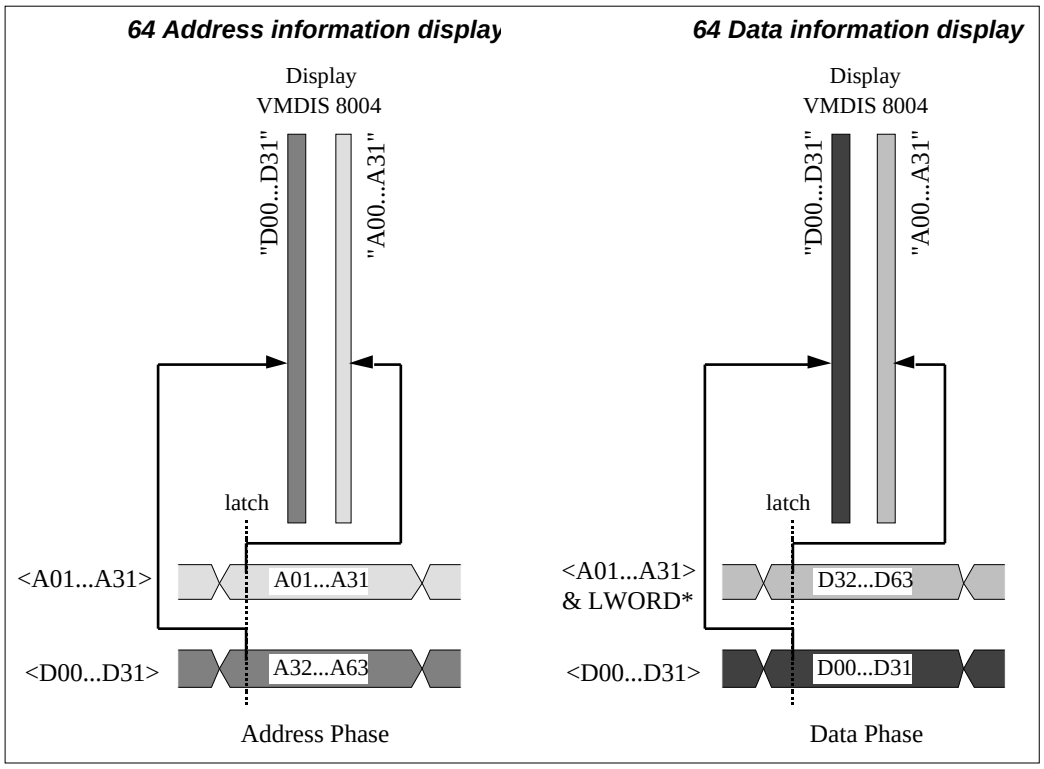

Fig 2.2

2.3 Stretched Signals

Due to their short duration, some signals have been stretched to allow the user to detect their presence.

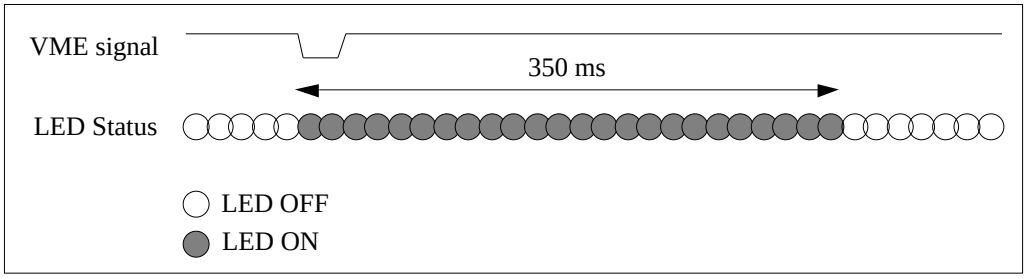

Fig 2.3

This is the case for the following signals:

AS* this signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals occurrence of VME cycle.

SYSRESET* this signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals presence of System Reset in the VME crate.

SYSFAIL* this signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals presence of System Failure in the VME rack.

ACFAIL* this signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals presence of Power Supply Failure in the VME rack.

BR(0-3)* this signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals presence of VME master unit requesting the VME bus.

SYSCLK this signal is not latched but stretched to 1.5 µs for the front panel LED visibility. This flashing signals presence of System Clock (16 MHz) in the VME rack.

An additional LED named "LBTO" is implemented for signalling local bus time-out if the VMDIS 8004 is VME arbiter and aborts, with a BERR* generation, the current VME cycle not yet acknowledged after BTO delay.

2.4 VME SYSRESET Generator

The VMDIS 8004 issues a VME SYSRESET on the following conditions:

❶ At power-up if used as VME slot 1

❷ Through the front panel SRES push-button (SW4)

❸ Through the front panel LEMO 00 (NIM or TTL input level according to the position of jumper J12, minimum pulse length = 1.5 µs), if jumper J13 is set on RES (see § 2.7 and § 5.3)

❹ Under software control through the CSR0 Register (refer to § 4.2)

The RESET pulse generated over the VME backplane is calibrated at 250 ms.

Warning Take care that generating a RESET on VME from the VMDIS 8004 will perform a RESET on each module located in your crate.

2.5 VME Slot 1 Function

The VMDIS includes a VME Slot 1 function, which can be enabled by the front panel VMEC switch (DSW8). While this function is enabled, the LED "VMEC" is ON.

The VME Slot 1 function features:

❶ A central 4-level VME arbiter. PRI or RRS mode selectable by the front panel PRI / RRS DIP switch (DSW7)

❷ VME Bus time-out logic with time-out selectable (15 or 255 µs ± 1 µs) by the front panel LBTO DIP switch (DSW2)

❸ VME 16 MHz clock driver

❹ VME Power-up RESET generator

❺ IACK daisy-chain driver as VME specification

When the VMDIS 8004 is expected to be used as VME slot 1, it must be inserted in the slot n°1 of the VME crate.

2.6 VME Interrupt Generator

The VMDIS 8004 includes a VME interrupt generator. This INTG logic can be triggered by the front panel push-button INT (SW3), under software control through CSR0 register (refer to § 4.2) or by the LEMO 00 NIM or TTL input. The VME interrupt level and the Status / ID are selectable through jumpers as described below. Please refer to § 5.3 for jumpers location.

The three jumpers INTL0...INTL3 allow the user to encode the level on which the VME Interrupt will be generated on VME (1 to 7). The Interrupt Level encoded by the jumpers can be read back by software in the CSR1 register (refer to § 4.2).

The eight remaining jumpers (STATUS ID) encode the value of the Interrupt Vector associated to the interrupt generated. The value of the Interrupt Vector can be read back in the CSR1 register (refer to § 4.2).

Interrupt Level and Interrupt Vector Setting

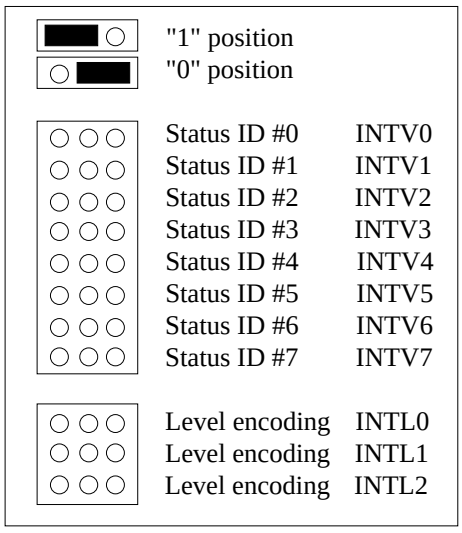

Fig 2.4

When the interrupt is pending, the LED INTP on the front panel is lit ON.

2.7 Front Panel LEMO Connector

The front panel LEMO 00 connector allows the generation of a VME SYSRESET (§ 2.5) or a VME Interrupt (§ 2.6) controlled by an external (negative logic) TTL or NIM signal.

The selection of the input signal (TTL or NIM) and of the signal generated (SYSRESET or Interrupt) is assumed by jumper J12 and J13 respectively as depicted in figure 2.5.

Input Signal Level and Signal Generation Selection

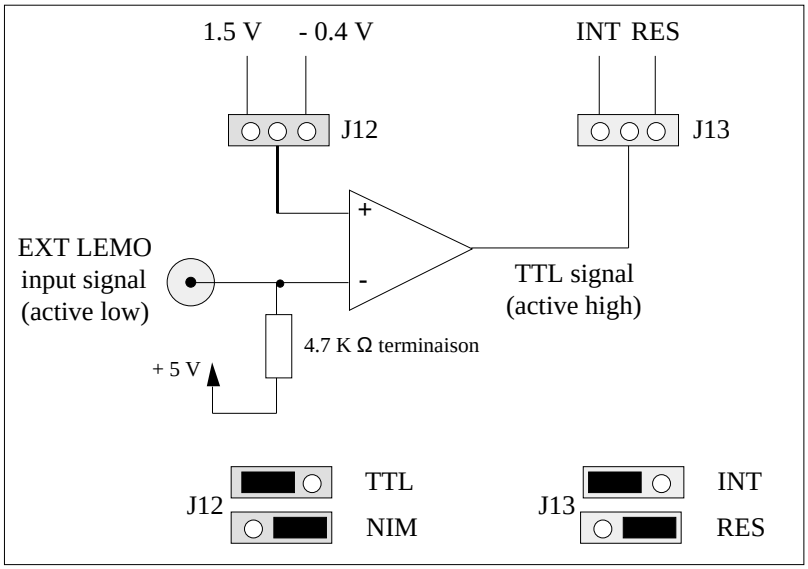

Fig 2.5

Warning The input signal is terminated with a 4.7 KΩ resistor to + 5 V. If no signal is input on the EXT LEMO, the comparator's output is inactive whatever the position of J12.

If you want to use NIM level input, you have to add an external resistor (50 Ω to ground).

2.8 Monitor Function

This function can only be used when the VMDIS 8004 is in VME mode.

This mode allows the user to access the VMDIS 8004 in Read, Write, BLT, ... through its VME slave interface as any other VME module. The VMDIS 8004 then answers with a DTACK (which delay in regard to the DS is software programmable) to any cycle containing an AM code equal to $14.

DS to DTACK Delay

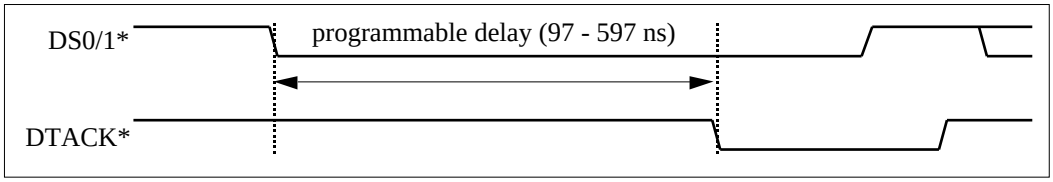

Fig 2.6

The MONitor mode can be selected by the front panel SELect switch when the VMDIS is in VME mode. It is also possible to force the VMDIS in MONitor mode through the VME A16 slave port by writing in the CSR0 register. The value of this delay is set by bits <12...15> in steps of 31.25 ns (see § 4.2).

The data read on Read cycles are not significant. This mode of operation provides a VME Slave device responding to all kind of VME cycles. As for regular mode of operation the VMDIS catches all parameters of the VME cycle whose can be read back and checked.

3. VSB DISPLAY MODE

3.1 VSB Cycle Memorisation

The VSB cycles signals are temporary memorised in registers with strobes related to the VSB cycle. The VSB cycles are caught whatever the VMDIS 8004 is in VSB or VME mode.

❶ When the VMDIS 8004 is in DIRect mode, the catching register are set in transparent and every cycle is displayed.

❷ When the VMDIS 8004 is in LATched mode, every VSB cycle is caught and displayed.

Every VSB signals is caught at specific time depending its meaning in the VSB cycles. The catching is done only when the VMDIS 8004 is in LATched mode.

3.2 Stretched Signals

Due to their short duration, some signals have been stretched to allow the user to detect their presence.

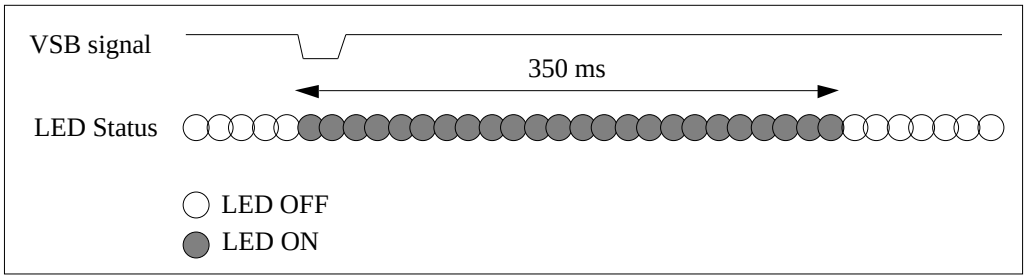

Fig 3.1

This is the case for the following signals:

PAS*	This signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals occurrence of VSB cycle.
WAIT*	This signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals presence of WAIT* in VSB cycle.
IRQ*	This signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals VSB Interrupt occurrence.
BREQ*	This signal is not latched but stretched to 350 ms for the front panel LED visibility. This flashing signals presence of VSB master unit requesting the VSB.
GA2-GA0	These signals are not latched because they are anyway static information.

An additional LED named " ADER" for address error is ON if the current VSB cycle is not decoded (If ASACK* 1, 0 = 00 when AC is going high).

3.3 VSB Central Arbiter

The VMDIS includes a VSB central arbiter, which is enabled only when the VMDIS is plugged in a VSB slot 0 (VSB geographic) and when the jumper J15 is set. While the VMDIS acts as VSB central arbiter, the LED "VSBC" is ON.

4. INTERNAL RESOURCES

4.1 VME Slave Base Address

The VMDIS 8004 occupies a 256 bytes area in the VME Short I/O A16. The base address is user selectable through 2 hex rotary switches located between the two VME / VSB connectors P1 and P2.

VME Short A16

A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
VME Base Address								Internal Registers Addressing							

The VMDIS 8004 can also act as VME interrupter, and therefore answers appropriately on VME IACK cycle (refer to § 2.6).

4.2 Internal Register Mapping

The VMDIS 8004 includes 16 internal 16-bit registers mapped as follows in the VME A16.

base + 0x0	VMEDATL	VME data low register
base + 0x2	VMEDATH	VME data high register
base + 0x4	VMEADDL	VME address low register
base + 0x6	VMEADDH	VME address high register
base + 0x8	VMESTA0	VME status register #0
base + 0xA	VMESTA1	VME status register #1
base + 0xC	BLTCNT	Block transfer counter register
base + 0xE	TIMCNT	Cycle duration counter register
base + 0x10	VSBDATL	VSB data low register
base + 0x12	VSBDATH	VSB data high register
base + 0x14	VSBADDL	VSB address low register
base + 0x16	VSBADDH	VSB address high register
base + 0x18	VSBSTA0	VSB status register #0
base + 0x1A	VSBSTA1	VSB status register #1
base + 0x1C	CSR0	Control & Status register
base + 0x1E	CSR1	VME Vector and interrupt level jumpers

VMEDATL Register (VME Data Low) - base + 0x0

This Read Only register provides the lowest data bytes of the last memorised VME transaction.

Bit <00>	VME Data #0
Bit <01>	VME Data #1
Bit <02>	VME Data #2
Bit <03>	VME Data #3
Bit <04>	VME Data #4
Bit <05>	VME Data #5
Bit <06>	VME Data #6
Bit <07>	VME Data #7
Bit <08>	VME Data #8
Bit <09>	VME Data #9
Bit <10>	VME Data #10
Bit <11>	VME Data #11
Bit <12>	VME Data #12
Bit <13>	VME Data #13
Bit <14>	VME Data #14
Bit <15>	VME Data #15

VMEDATH Register (VME Data High) - base + 0x2

This Read Only register provides the highest data bytes of the last memorised VME transaction.

Bit <00>	VME Data #16
Bit <01>	VME Data #17
Bit <02>	VME Data #18
Bit <03>	VME Data #19
Bit <04>	VME Data #20
Bit <05>	VME Data #21
Bit <06>	VME Data #22
Bit <07>	VME Data #23
Bit <08>	VME Data #24
Bit <09>	VME Data #25
Bit <10	VME Data #26
Bit <11	VME Data #27
Bit <12	VME Data #28
Bit <13	VME Data #29
Bit <14	VME Data #30
Bit <15	VME Data #31

VMEADDL Register (VME Address Low) - base + 0x4

This Read Only register provides the lowest address bytes of the last memorised VME transaction.

Bit <00>	0 in VME D32 or VME A64 mode LWord* in VME D64 mode.
Bit <01>	VME Address #1
Bit <02>	VME Address #2
Bit <03>	VME Address #3
Bit <04>	VME Address #4
Bit <05>	VME Address #5
Bit <06>	VME Address #6
Bit <07>	VME Address #7
Bit <08>	VME Address #8
Bit <09>	VME Address #9
Bit <10>	VME Address #10
Bit <11>	VME Address #11
Bit <12>	VME Address #12
Bit <13>	VME Address #13
Bit <14>	VME Address #14
Bit <15>	VME Address #15

VMEADDH Register (VME Address High) - base + 0x6

This Read Only register provides the highest address bytes of the last memorised VME transaction.

Bit <00>	VME Address #16
Bit <01>	VME Address #17
Bit <02>	VME Address #18
Bit <03>	VME Address #19
Bit <04>	VME Address #20
Bit <05>	VME Address #21
Bit <06>	VME Address #22
Bit <07>	VME Address #23
Bit <08>	VME Address #24
Bit <09>	VME Address #25
Bit <10>	VME Address #26
Bit <11>	VME Address #27
Bit <12>	VME Address #28
Bit <13>	VME Address #29
Bit <14>	VME Address #30
Bit <15>	VME Address #31

VMESTA0 Register (VME Status 0) - base + 0x8

This Read Only register provides signals of the VME protocol relative to the last memorised VME transaction.

Bit <00>	VME Address Modifier #0
Bit <01>	VME Address Modifier #1
Bit <02>	VME Address Modifier #2
Bit <03>	VME Address Modifier #3
Bit <04>	VME Address Modifier #4
Bit <05>	VME Address Modifier #5
Bit <06>	VME LWORD
Bit <07>	VME AS (asserted during 350 ms only)
Bit <08>	VME DS0
Bit <09>	VME DS1
Bit <10>	VME WRITE
Bit <11>	VME DTACK
Bit <12>	VME BERR
Bit <13>	VME RETRY
Bit <14>	VME LBTO
Bit <15>	VME ACFAIL (asserted during 350 ms only)

VMESTA1 Register (VME Status 1) - base + 0xA

This Read Only register provides additional signals of the VME protocol relative to the last memorised VME transaction.

Bit <00>	VME BREQ0 (asserted during 350 ms only)
Bit <01>	VME BREQ1
Bit <02>	VME BREQ2
Bit <03>	VME BREQ3
Bit <04>	VME BBSY (filtered)
Bit <05>	VME IACK
Bit <06>	VME IRQ1
Bit <07>	VME IRQ2
Bit <08>	VME IRQ3
Bit <09>	VME IRQ4
Bit <10>	VME IRQ5
Bit <11>	VME IRQ6
Bit <12>	VME IRQ7
Bit <13>	Not used, read as 0
Bit <14>	Not used, read as 0
Bit <15>	STOP (VMDIS internal state)

BLTCNT Register (Block Transfer Counter Register) - base + 0xC

This Read Only register holds the value of the block transfer counter. An internal logic counts in VME or VSB cycles, the number of data strobes. The bus (VME or VSB) for which this logic is active is selectable through bit <10> of the CSR0 register.

At the beginning of each VME or VSB cycle accepted (front edge of AS*), the counter is cleared. On every front edge of the data strobe DS*, the counter is then incremented. By default, the logic is protected against roll-over if the DS* number exceeds 255 (then you always read BLTCNT register to 0). But you can let the counter free running by selecting the bit <07> in the CSR0 register. This feature has been added to be used with the VME D64 mode. In this case, you can generate block transfer of 256 * 64 bits-words. As a first DS* edge is generating during the address phase, you obtain then 257 data strobes.

If a first reading of the BLTCNT register (with no free running) gives a result of 0, it may report a burst of 255 or 256 words. So, you can set the BLTCNT counter free running and perform again the same transfer to determine now the exact transfer length:

Reading 255 corresponds to 254 words
Reading 0 corresponds to 255 words
Reading 1 corresponds to 256 words

The control logic is not triggered by the VME cycles used to access internal VMDIS 8004 registers. This feature can be used to verify the burst length of VME / VSB transfers.

Bit <00>	BLTCNT0
Bit <01>	BLTCNT1
Bit <02>	BLTCNT2
Bit <03>	BLTCNT3
Bit <04>	BLTCNT4
Bit <05>	BLTCNT5
Bit <06>	BLTCNT6
Bit <07>	BLTCNT7
Bit <08>	Undefined, could be 0 or 1
Bit <09>	Undefined, could be 0 or 1
Bit <10>	Undefined, could be 0 or 1
Bit <11>	Undefined, could be 0 or 1
Bit <12>	Undefined, could be 0 or 1
Bit <13>	Undefined, could be 0 or 1
Bit <14>	Undefined, could be 0 or 1
Bit <15>	Undefined, could be 0 or 1

TIMCNT Register (Cycle Time Counter Register) - base + 0xE

This Read Only register holds the value of cycle measurement counter. An internal logic allows the measurement of a VME or VSB cycle duration. The bus (VME or VSB) for which this logic is active is selectable through bit <10> of the CSR0 register.

At the beginning of each VME or VSB cycle accepted (front edge of AS*), the counter is cleared and counts (at a 32 MHz frequency) until the end of AS*. The logic allows cycle duration measurements from 62.5 ns up to 128 µs incremented in steps of 31.25 ns and with a global precision of ± 31.25 ns . The control logic is not triggered by the VME cycles used to access internal VMDIS 8004 registers.

The cycle duration can be calculated with the following formula:

t_{cycle} = [TIMCNT + 2] x 31.25 ± 31.25 [ns]

Bit <00>	TIMCNT0
Bit <01>	TIMCNT1
Bit <02>	TIMCNT2
Bit <03>	TIMCNT3
Bit <04>	TIMCNT4
Bit <05>	TIMCNT5
Bit <06>	TIMCNT6
Bit <07>	TIMCNT7
Bit <08>	TIMCNT8
Bit <09>	TIMCNT9
Bit <10>	TIMCNT10
Bit <11>	TIMCNT11

Note This counter is not free running. It goes from "FFF" to "0" then stop counting. So, if the transfer exceeds 128 µs, you always read this TIMCNT register to 0.

Bit <12>	SELCNT (status of CSR0 bit <10>). This bit allows a check of the source of the BLTCNT and TIMCNT. SELCNT = 0 VME cycle SELCNT = 1 VSB cycle
Bit <13>	VME RRS Arbitration mode status
Bit <14>	BERR STOP mode status
Bit <15>	IACK STOP mode status

VSBDATL Register (VSB Data Low) - base + 0x10

This Read Only register provides the lowest data bytes of the last memorised VSB transaction.

Bit <00>	VSB Data #0
Bit <01>	VSB Data #1
Bit <02>	VSB Data #2
Bit <03>	VSB Data #3
Bit <04>	VSB Data #4
Bit <05>	VSB Data #5
Bit <06>	VSB Data #6
Bit <07>	VSB Data #7
Bit <08>	VSB Data #8
Bit <09>	VSB Data #9
Bit <10>	VSB Data #10
Bit <11>	VSB Data #11
Bit <12>	VSB Data #12
Bit <13>	VSB Data #13
Bit <14>	VSB Data #14
Bit <15>	VSB Data #15

VSBDATH Register (VSB Data High) - base + 0x12

This Read Only register provides the highest data bytes of the last memorised VSB transaction.

Bit <00>	VSB Data #16
Bit <01>	VSB Data #17
Bit <02>	VSB Data #18
Bit <03>	VSB Data #19
Bit <04>	VSB Data #20
Bit <05>	VSB Data #21
Bit <06>	VSB Data #22
Bit <07>	VSB Data #23
Bit <08>	VSB Data #24
Bit <09>	VSB Data #25
Bit <10>	VSB Data #26
Bit <11>	VSB Data #27
Bit <12>	VSB Data #28
Bit <13>	VSB Data #29
Bit <14>	VSB Data #30
Bit <15>	VSB Data #31

VSBADDL Register (VSB Address Low) - base + 0x14

This Read Only register provides the lowest address bytes of the last memorised VSB transaction.

Bit <00>	VSB Address #0
Bit <01>	VSB Address #1
Bit <02>	VSB Address #2
Bit <03>	VSB Address #3
Bit <04>	VSB Address #4
Bit <05>	VSB Address #5
Bit <06>	VSB Address #6
Bit <07>	VSB Address #7
Bit <08>	VSB Address #8
Bit <09>	VSB Address #9
Bit <10>	VSB Address #10
Bit <11>	VSB Address #11
Bit <12>	VSB Address #12
Bit <13>	VSB Address #13
Bit <14>	VSB Address #14
Bit <15>	VSB Address #15

VSBADDH Register (VSB Address High) - base + 0x16

This Read Only register provides the highest address bytes of the last memorised VSB transaction.

Bit <00>	VSB Address #16
Bit <01>	VSB Address #17
Bit <02>	VSB Address #18
Bit <03>	VSB Address #19
Bit <04>	VSB Address #20
Bit <05>	VSB Address #21
Bit <06>	VSB Address #22
Bit <07>	VSB Address #23
Bit <08>	VSB Address #24
Bit <09>	VSB Address #25
Bit <10>	VSB Address #26
Bit <11>	VSB Address #27
Bit <12>	VSB Address #28
Bit <13>	VSB Address #29
Bit <14>	VSB Address #30
Bit <15>	VSB Address #31

VSBSTA0 Register (VSB Status 0) - base + 0x18

This Read Only register provides signals of the VSB protocol relative to the last memorised VSB transaction.

Bit <00>	VSB SPACE0
Bit <01>	VSB SPACE1
Bit <02>	VSB SIZ0
Bit <03>	VSB SIZ1
Bit <04>	VSB ASACK0
Bit <05>	VSB ASACK1
Bit <06>	VSB LOCK
Bit <07>	VSB PAS during 350 ms only
Bit <08>	VSB DS
Bit <09>	Not used, read as 0
Bit <10>	VSB Write
Bit <11>	VSB ACK
Bit <12>	VSB ERR
Bit <13>	VSB CACHE
Bit <14>	VSB ADDRESS ERROR
Bit <15>	VME ACFAIL during 350 ms

VSBSTA1 Register (VSB Status 1 - base + 0x1A

This Read Only register provides additional signals of the VSB protocol relative to the last memorised VSB transaction.

Bit <00>	VSB BREQ (Direct from backplane, during 350 ms)
Bit <01>	Not used, read as 0
Bit <02>	Not used, read as 0
Bit <03>	Not used, read as 0
Bit <04>	VSB BBSY (not filtered)
Bit <05>	Not used, read as 0
Bit <06>	VSB IRQ, during 350 ms
Bit <07>	Not used, read as 0
Bit <08>	Not used, read as 0
Bit <09>	Not used, read as 0
Bit <10>	GA0
Bit <11>	GA1
Bit <12>	GA2
Bit <13>	VSB AC
Bit <14>	VSB WAIT, during 350 ms
Bit <15>	STOP (VMDIS internal state)

CSR0 Register (Control and Status 0)- base + 0x1C

This register is Read / Write. The bits <03...00> are Read only, the bits <15...08> are Write only, the bits <07...04> are Read / Write.

❶ Status information

When bits <07...00> are read, they contain following information:

Bit <00> VME / VSB front panel switch status

0 VME selected
1 VSB selected

Bit <01> LATched mode status

Bit <02> MONitor mode status

Bit <03> DIRect mode status

Bit <04> VME A64 mode status

Bit <05> VME D64 mode status

Note If bits <04...05> are set simultaneously, the VMDIS 8004 is in D64 mode; it displays the whole 64 data bits on Address and Data LEDs.

Bit <06> VME Slot 1 (System controller status)

0 VMDIS is not VME System Controller
1 VMDIS is VME System Controller

Bit <07> VSB Slot 0

0 VMDIS is not VSB Slot 0
1 VMDIS is VSB Slot 0

❷ Control bits

Bits <15...04> are used for commands (When written)

Bit <04> VME A64 mode (if DIP Switch DSW5 is let in A32 position)

0 A32 mode
1 A64 mode

Bit <05> VME D64 mode (if DIP Switch DSW6 is let in D32 position)

0 D32 mode
1 D64 mode

Bit <06> INTG

By asserting a positive pulse (setting 1 then 0) on this line, you generate a VME Interrupt (ref. § 2.6 for level and status ID encoding)

Bit <07> BLTCNT free running (refer BLTCNT register)

0 BLTCNT counter is protected against roll-over if it exceeds 255
1 BLTCNT is free running

Bits <09...08>	These 2 bits allow the user to put the VMDIS 8004 in different modes 00 No action 01 Puts the VMDIS in LATched mode 10 Puts the VMDIS in DIRect mode 11 Puts the VMDIS in MONitor mode
Bit <10>	This bit allows the control of the source of the BLTCNT and TIMCNT. This status can be read back in the TIMCNT register bit <12> SELCNT = 0 VME cycle monitored = 1 VSB cycle monitored
Bit <11>	This bit allows the generation of a VME SYSRESET, if the jumper J14 is set. By setting this bit to 1, a VME SYSRESET is generated (calibrated pulse). Take special care with this feature!
Bits <15...12>	DEL3...DEL0 DTACK* programmable delay for MONitor mode (refer to § 2.8 and to the following table)

Correspondence between the coding of bits <15...12> and the physical DS to DTACK Delay

DEL code	*DS ➠ DTACK delay [ns]*	
	Write	Read
1111	96.75	128
1110	128	159.25
1101	159.25	190.5
1100	190.5	221.75
1011	221.75	253
1010	253	284.25
1001	284.25	315.5
1000	315.5	346.75
0111	346.75	378
0110	378	409.25
0101	409.25	440.5
0100	440.5	471.75
0011	471.75	503
0010	503	534.25
0001	534.25	565.5
0000	565.5	596.75

Those values are given with a precision of + 60.5 ns, - 0 ns.

CSR1 register (Control and Status 1) - base + 0x1E

This Read only register allows the user to read the interrupt related status ID set on the board by jumpers (refer to § 2.6 and § 5.3).

Bit <00>	VME Status ID #0 (jumper status)
Bit <01>	VME Status ID #1 (jumper status)
Bit <02>	VME Status ID #2 (jumper status)
Bit <03>	VME Status ID #3 (jumper status)
Bit <04>	VME Status ID #4 (jumper status)
Bit <05>	VME Status ID #5 (jumper status)
Bit <06>	VME Status ID #6 (jumper status)
Bit <07>	VME Status ID #7 (jumper status)
Bit <08>	VME Interrupt level #0 (jumper status)
Bit <09>	VME Interrupt level #1 (jumper status)
Bit <10>	VME Interrupt level #2 (jumper status)
Bit <11>	INTP. Interrupt pending status
Bit <12...15>	Undefined, could be 0 or 1

5. INSTALLATION NOTES

5.1 Front Panel Display

VME / VSB LEDs Assignments

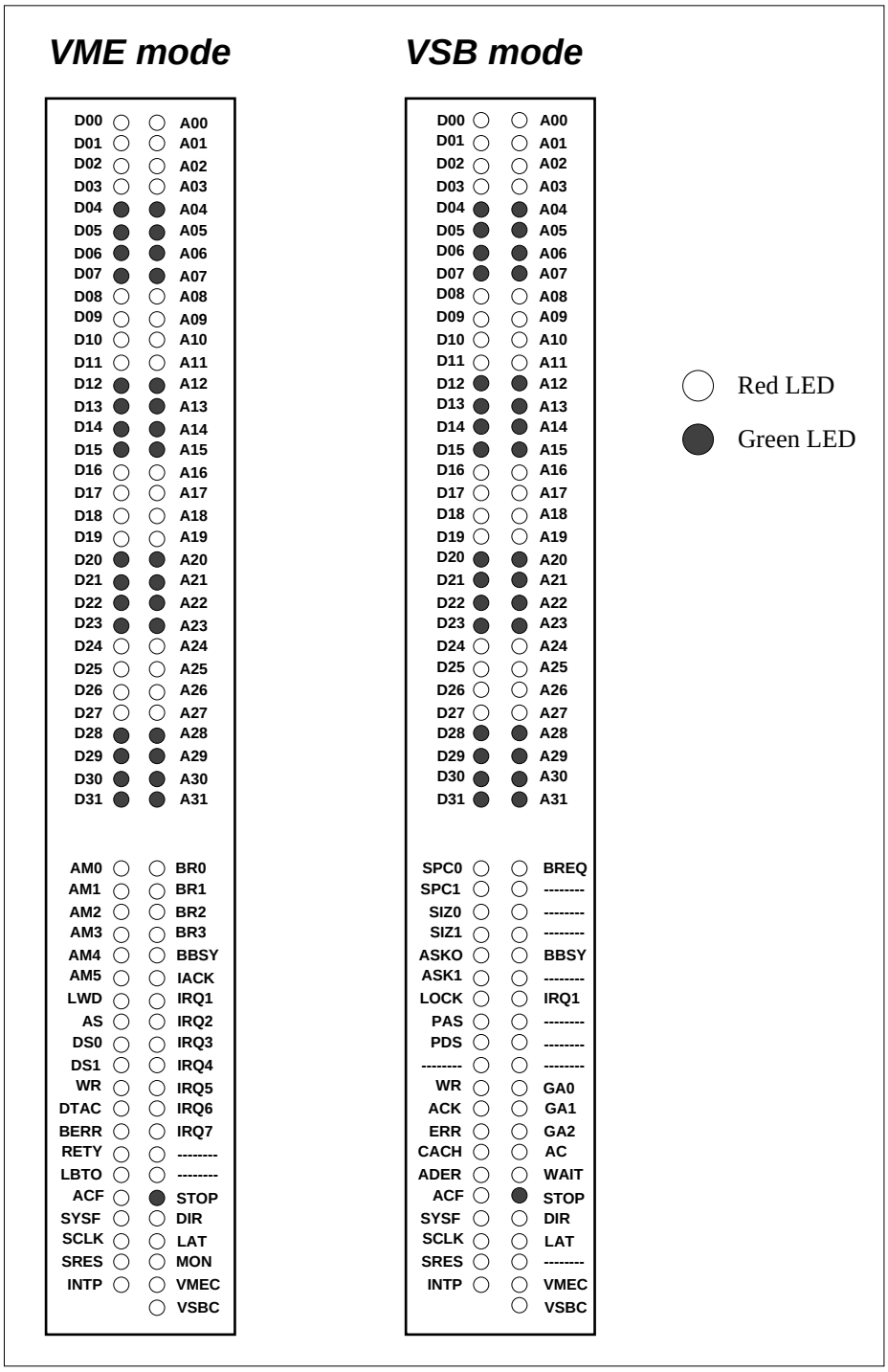

Fig 5.1

The lowest half of the LEDs may report different information, depending on the mode selected (VME or VSB). In this case, a double serigraphy is implemented for the concerned LEDs: black for VME information, red for VSB information (for example, black for AM0 and red for SPC0). If the signals are the same in both modes, the names are printed in black (WR for instance is printed in black). If the signal is relevant for one mode only, its name is printed in black for a VME signal and in red for a VSB signal (for example BR2 printed in black and AC printed in red).

5.2 Front Panel Switches

Switches Location

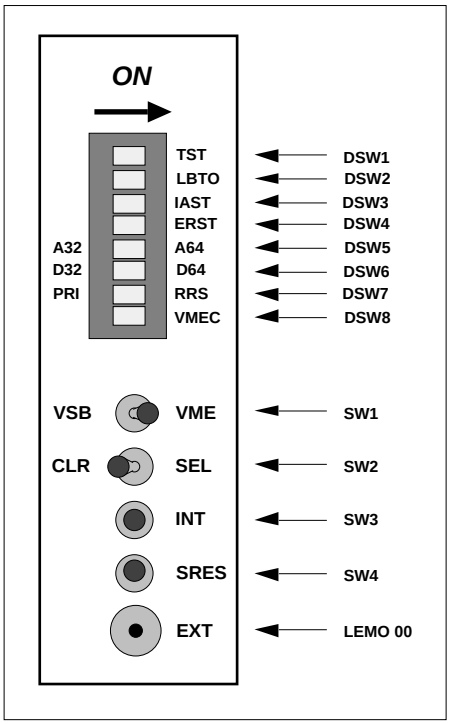

Fig 5.2

Front Panel Static Option (mini-DIP switches)

DSW1	TST	When ON, displays the value of register TIMCNT on the address LEDs "A00...A15", and the value of register BLTCNT on the address LEDs "A16...A31" (see § 4.2).
DSW2	LBTO	Short (15 µs) / Long (255 µs) VME BTO (see § 2.5). Switch ON: Long VME BTO mode
DSW3	IAST	Stop on IACK cycle (see § 1.6)
DSW4	ERST	Stop on ERROR cycle (see § 1.6)
DSW5	A32 / A64	VME A32 / A64 address display selection (see § 2.2)
DSW6	D32 / D64	VME D32 / D64 data display selection (see § 2.2)
DSW7	PRI / RRS	VME PRI / RRS arbitration selection (see § 2.5). Switch ON: RRS mode
DSW8	VMEC	VME System controller enable (see § 2.5)

Front Panel Command switch

SW1	VME / VSB	Two positions switch selecting the VME or VSB display
		LEFT VSB displayed RIGHT VME displayed
SW2	CLR / SEL	Three positions push switch (right, left and centre)
		LEFT Clears the display and disables STOP mode RIGHT Mode selection (LAT, DIR, MON) CENTER No action
SW3	INT	VME interrupt generation push-button
SW4	SRES	VME System RESET push-button

Front Panel Connector

LEMO 00	EXT	VME Interrupt or SYSRESET* (depending on J15 jumper position) negative input NIM or TTL level (selected with J14 jumper), terminated with a 4.7 KΩ to + VCC.

5.3 Jumpers Location and Setting

J1...J3	INTL	Interrupt Level encoding (refer to § 2.6)
J4...J11	INTV	Interrupt Vector encoding (refer to § 2.6)
J12	TTL / NIM	Selection of the level (TTL / NIM) of the signal input on the front panel LEMO 00 connector (refer to § 2.7)
J13	INT / RES	Selection of the type of VME signal (Interrupt or SYSRESET) generated on the VME backplane when a TTL or NIM signal is input on the front panel LEMO 00 connector (refer to § 2.7)
J14	SRES	When plugged in, allows the propagation of a VME SYSRESET generated by software through CRS0 on the VME backplane (refer to § 4.2)
J15	VSB0	When plugged in, configures the VMDIS 8004 as VSB Central Arbiter (refer to § 3.3)

Jumpers Location

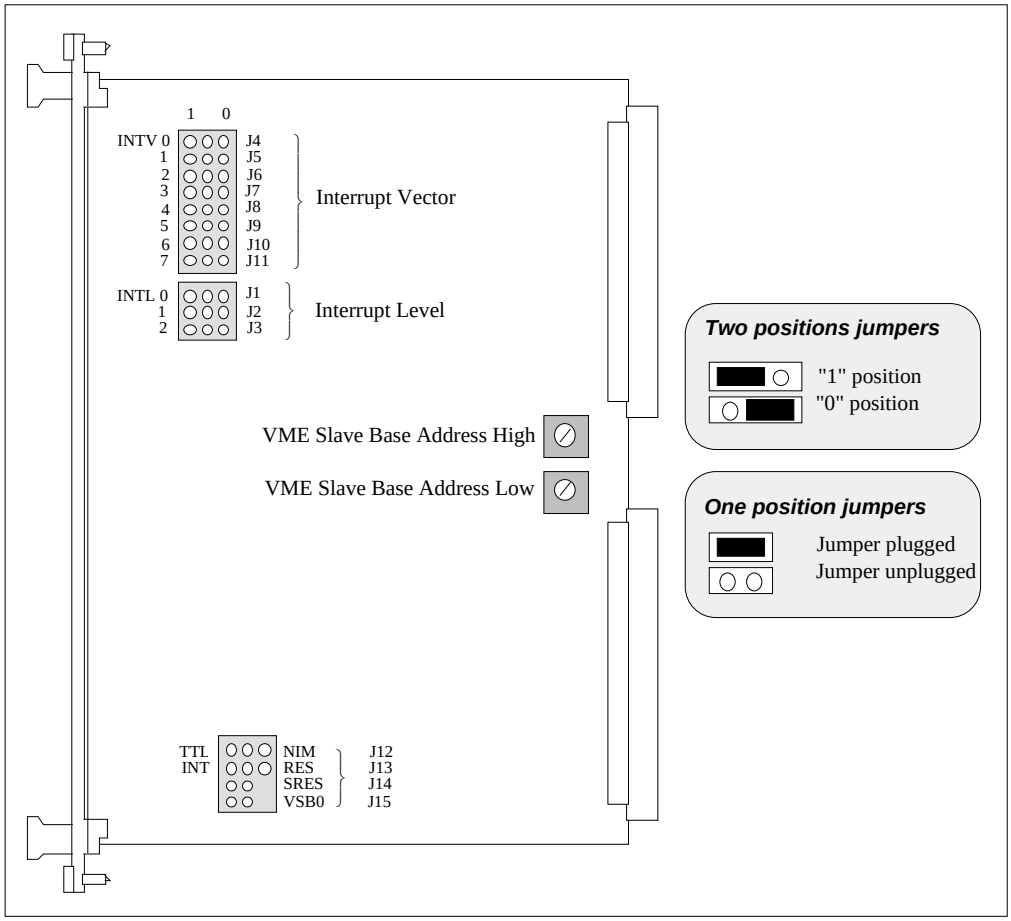

Fig 5.3