STR610/CBV
CAMAC to VSB Interface
Technical Manual

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1 INTRODUCTION

The CAMAC to VSB interface is a single width CAMAC Crate Controller (CC) driven from the VME Subsystem Bus (VSB) via the VSB Differential Cable (VDC). The specification of STR610/CBV is similar to A1 Type crate controllers. More than one CC in one CAMAC crate is not allowed. CBV occupies the station N=24 and requires a connection to station N=25 via another CAMAC module e.g. STR611/DMS. CBV maps a portion of VSB address space to CAMAC C, N, A, F and generates single CAMAC cycles from each proper VSB cycle. Up to 15 STR610/CBV modules (15 CAMAC crates) can be connected to one VDC. There is no memory on STR610/CBV board and for this reason DMA and block transfer is not supported.

2 SYSTEM OVERVIEW, HARDWARE REQUIREMENTS

The hardware components require for interfacing of VME to CAMAC over VSB, differential cable and STR610/CBV are:

- VME:
  The VME crate with both J1 and J2 backplane. The J2 backplane with a 96-pin connector at the rear side, the crate must accept Euro-boards of 10cm dimensions.

- VSC Module:
  The VSC module (a VSB to differential bus interface) to be placed in VME crate from rear side connected to J2 backplane.

- VDC Cable:
  VSB Differential Bus (VDC) connects VSC module, placed in VME crate, with STR610/CBV module(s) in CAMAC crate(s); max. length 50 meters.

- CAB Extension Board:
  If more than one STR610/CBV module should be connected to VDC, then a CAB extension board is needed.

- TER Termination board:
  The VDC must be terminated at both ends with TER (termination) board.

- STR611/DMS Module:
  The coded CAMAC N lines from CBV module must be connected over ACB (40-strip flat cable at the rear of CAMAC module) to CAMAC station N=25 to STR611/DMS display and dummy module.

3 FUNCTIONAL DESCRIPTION

The STR610/CBV module transform VSB cycle to CAMAC cycle. It maps portion of VSB address space to CAMAC **C, N, A, F**, where:

C CAMAC crate no. C=1 to 15,
N CAMAC station no. N=1 to 24,
F CAMAC function F=0 to 31
A CAMAC subaddress A=0 to 15.

The incoming differential control signals are converted to TTL level at transceivers. The VSB address and data are multiplexed, so each transfer cycle has two phases; address phase and data phase. At address phase the actual address, corresponding to CAMAC C, N, A, F is clocked to CBV address register and the crate number is compared with address bits 21-24. If crate number match then at data phase the CAMAC cycle is generated and the data is send from VSB to CAMAC while VSB write cycle or from CAMAC to VSB while VSB read cycle. The data transfer size is always 32 bit parallel. The data bit 25 to 31 are read as 0.

3.1 VSB TRANSFER CYCLE

The control signals of CBV module correspond to VSB. There are 6 control signals PAS, ASCK, DS, ACK, WR, IRQ.

3.2 CBV DATA FORMAT

CANAC data is 24 bit of width, and VSB long word data is of 32 bit width. At read cycle the most significant byte is set to 0. At write cycle the most significant byte is ignored.

CBV Data Layout

31 28	24	20	16	12	8	4	0	Offset
QXOO	OOOO	DDDD	DDDD	DDDD	DDDD	DDDD	DDDD	0

Q - read as zero or as CAMAC Q response when enabled.
X - read as zero or as CAMAC X response when enabled.
O - always zero.
D - CAMAC data

4 ADDRESSING OVERVIEW

4.1 DATA TRANSFER SIZE

Data transfer size over VSB-CBV connection is 32 bit parallel (long word) only. The two low significant address bits are always 0 so the last hexadecimal address digit can be 0, 4, 8 or C.

4.2 VSB WINDOWS

There are six user VSB windows W1 - W6, selected on the VSC board and corresponding to address bits no.: 26, 27, 28. (W1 selected, bit 26-28=000). Each window overlaps 64 Mbyte address space. Switching window W1 on, the address space 0 to 3FFFFC is selected. Switching window W2 on, the address space 400000 to 7FFFFC is selected. Switching window W! and W2 on, the address space 0 to 7FFFFC is selected.

4.3 CAMAC CRATE NUMBER

Up to 15 CAMAC crates can be connected to one VSB interface (VSC module). The crate number can be selected at a hexadecimal rotary switch on the front of CBV module. Crate number C can be in the range from C=1 to C=15. The selected crate number is displayed at the front panel, too. Crate number 0 is reserved for future use.

4.4 CBV ADDRESS LAYOUT

CBV Address Layout

31 28	24	20	16	12	8	4	0	Offset
XXXW	WWXC	CCCX	XXXX	NNNN	NFFF	FFAA	AAOO	0

X - Not decoded (do not care).
W - VSB Window, decoded on VSC board.
C - CAMAC crate number on VSB selected on CBV board.
N - CAMAC station number
F - CAMAC function
A - CAMAC subaddress
O - always zero

4.5 MULTIPLE ADDRESSING

The bit no. 25 and 16 to 20 are not decoded on the STR610/CBV module so that multiple addressing occurs.

4.6 CVI COMPATIBILITY MODE

CVI CAMAC VSB Intelligent Interface is a 68030 CPU based CAMAC readout processor. The CVI decodes address bit no. 20 to 16 and it can be used in CBV mode. For software compatibility it is usefull to address both module types with corresponding offset. For all CAMAC **N, A, F** bit no. 20 to 16 shall be (hex. 18), for Status Register bit no. 20 to 16 shall be (hex. 1b).

4.7 CAMAC N, A, F ADDRESS SPACE

The valid CAMAC address begin with **N(1)F(0)A(0)** (hex. 0800) and ends with **N(24)F(31)A(15)** (hex. C7FC). Some additional addresses are decode internal to CBV, for more details see "CAMAC special functions" section.

4.8 BUS ERROR (TIME OUT)

Bus error occurs while addressing of non existent crate number, not valid CAMAC address, or while writing to CAMAC read function **F(0)-F(7)** or while reading from CAMAC write function **F(16)-F(23).**

5 CAMAC SPECIAL FUNCTIONS

The STR610/CBV module decodes some VSB addresses as internal functions:

•	CAMAC INIT **N(28)F(26)A(8),** (hex. E6A0)
•	CAMAC CLEAR **N(28)F(26)A(9),** (hex. E6A4)
•	ENABLE CAMAC **N(28)F(26) A(9),** (hex. F6A4)
•	DISABLE CAMAC INHIBIT **N(30)F(24)A(9),** (hex. F624)
•	ENABLE VSB interrupt request (IRQ) **N(30)F(26)A(10),** (hex. F6A8)
•	DISABLE VSB interrupt request (IRQ) **N(30)F(24)A(10),** (hex. F628)
•	ENABLE X and Q readout **N(28)F(26)A(1),** (hex. E684)
•	DISABLE X and Q readout **N(28)F(24)A(1),** (hex. E604)
•	STATUS REGISTER **N(28)F(27)A(0),** (hex. E6C0)

The selection of other addresses as above will cause a VSB timeout.

5.1 CAMAC INIT (Z)

CAMAC INIT function generated while addressing 6EA0 hex or **N(28)F(26)A(8)** executes a CAMAC cycle with B, S1, S2 and Z signals active. The INIT function activates the CAMAC INHIBIT Flip-Flop.

5.2 CAMAC CLEAR (C)

CAMAC CLEAR function generated while addressing 6EA4 hex or **N(28)F(26)A(9)** executes a CAMAC cycle with B, S1, S2 and C signals active.

5.3 CAMAC INHIBIT (I)

Addressing F624 or **N(30)F(26)A(9**) enables the inhibit Flip-Flop (F-F), so the CAMAC INHIBIT line is set to the active state. Addressing F6A4 or **N(30)F(24)A(9)** disables the inhibit F-F. The CAMAC INIT function activates the INHIBIT F-F. This function does not generate any CAMAC cycle.

5.4 CAMAC LAM, VSB INTERRUPT LOGIC

The enable-disable-VSB-interrupt Flip-Flop and CAMAC LAM signal L1 are connected to VSB interrupt request line. Addressing F6A8 or **N(30)F(26)A(10)** enables VSB interrupt from LAM no. 1, the function **N(30)F(24)A(10)** or address F628 disables VSB interrupt request but doen‘t clear the LAM source which must be cleared separately. After power up the VSB interrupt request is disabled.

5.5 ENABLE Q AND X RESPONSE

CAMAC function **N(28)F(26)A(1),** (hex. E684) enables Q response to be readout as data bit 31 and X response as bit 30. Function **N(28)F(24)A(1),** (hex. E604) disables such a readout and data bits 31 and 30 will be read as zero. Independent of this functions Q and X response can be readout from the Status Register.

5.6 CAMAC X, Q RESPONSE

Bit no. 0 of Status Register corresponds to X response and bit no. 1 to Q. Both bits are active high, i.e. there was a response at the last CAMAC cycle if the bit is set to one. This function does not generate any CAMAC cycle.

5.7 STATUS REGISTER

The bit 0 to 3 of SR is used to obtain a hardware status of CBV, the SR bit 4 to 23 can be written and read. The address of SR is (hex. E6C0).

The Status Register

31 28	24	20	16	12	8	4	0	Offset
OOOO	OOOO	DDDD	DDDD	DDDD	DDDD	DDDD	RHQX	0

0 - always zero.
D - DATA, can be written and read.
R - if 1 then interrupt request to VSB is set.
H - if 1 then CAMAC inhibit is on.
Q - if 1 then there was Q- response at last CAMAC cycle.
X - if 1 then there was X- response at last CAMAC cycle.

6 CBV BOARD DESCRIPTION

6.1 FRONT PANEL

Front panel is composed of LED display, CAMAC crate select switch and 96-pin VDC connector.

- 4 LEDs for coded CAMAC crate no..
- 1 LED TERM. It is on when termination board (TER) is on.
- 1 LED IRQ. It is on when VSB interrupt request is set.
- 1 LED CYCLE. It is on while valid VSB cycle.
- 1 LED EQ. It is on while selected crate no. equals VSB crate no..

6.2 TECHNICAL DATA

STR610/CBV is a single-width CAMAC board. STR610/CBV module must occupy CAMAC station N=24. It requires connection to station N=25 via 40-wire flat cable type NCON to STR611/DMS module. This cable connects CAMAC ACB lines from STR610/CBV to STR611/DMS.

6.3 VSB TRANSFER RATE

VSB has a handshake bus protocol. For each transfer phase (address and data) acknowledge is send back from CBV to VSB master. That means that 6 times cable delay is added to each CAMAC (1µs) and VSB (duration depends on VSB master) cycle.

6.4 VDC DIFFERENTIAL BUS, VDC

The VDC is an 80-wire screened cable. Screen is connected to ground at one side. There are 96-pin connectors on both ends of VDC. VDC must be terminated on both ends with TER termination board.

6.5 POWER SUPPLY REQUIREMENTS AND POWER CONSUMPTION

The STR610/CBV requires less than 2,5 Amps. on +5V.

7 RELATED PRODUCTS

STR723	Differential VSB Extension
STR723/VDB	Differential Interconnect Round Cable (basic price)
STR723/CAB	Cable Adapter Board
STR725	VME to VSB Converter
STR610/CBV	CBV VME/VSB driven CAMAC Controller
STR611/DMS	CAMAC Dataway Display and Slot 25 Device for STR610/CBV
STR613/DUM	Slot 25 Device for STR610/CBV (includes one STR613/TERM Terminator)
STR613/TERM	Terminator for the STR613/DUM