A new Interlock Design for the TESLA RF System

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• The Problem
• The Interlock Architecture
• Implementation
• Status of the Project

Main Task of the Interlock System

--> to prevent any damage from the cost expensive components of the RF station
--> also to prevent any damage from other environment

Sources of Interlock Error Signals

• hard component failures (non-reversible hardware malfunction)
  --> broken cable or damaged contact, dead sensor, ...
• soft errors (e.g. sparks in the klystron or wave guide system,
  temperature above a threshold, ...)
• error conditions caused by transient noise from the RF station itself
Architecture of the existing Interlock

Strictly digital hierarchical Interlock

- Process Analysis
- Analog Process Input
  - Sensor
- Digital Process Input
  - Adapter Unit
- Output to Process
- Analog Output
  - Adapter Unit
  - Digital Output

Klystron, RF Station
**Klystron Interlock Inputs**

- **Digital Inputs**
  - Oil levels
  - Cooling water flow
  - Vacuum pump current

- **Analog Inputs**
  - Oil temperature
  - Cooling water temperature
  - Heater current
  - Solenoid current
  - SF6 gas pressure

**Klystron Interlock Inputs / Outputs**

- **Preprocessed Inputs**
  - Person interlock o.k.
  - RF leakage detector
  - Modulator ready
  - Gun interlock o.k.
  - RF system ready

- **Interlock Outputs**
  - Modulator on
  - Heater power supply on
  - Solenoid power supply on
  - RF enable
Response Times

- Ultra Fast (UF): \( R_t < 1 \mu s \)
- Fast (F): \( R_t = 1 ... 5 \mu s \)
- Slow (SL): \( R_t > 5 \mu s \)

--> Actual implementation only SL and F
--> ca. 40 signals to process

Overview over the new Interlock Design
The Implementation

Implementation Constraints

- **limited space in TESLA-tunnel**
  - combine Control & Interlock Functions into only one crate per RF-station
  - perform communication between modules via backplane
    (no extra cable for communication)
  - process-I/O with no cables to the front side of the crate; all cables from rear site

- **Other, DESY defined constraints**
  - **use a standard** with stable, fast enough & easy to implement bus interface
  - **use a standard** that gives flexibility at the level of system integration
    (definition of backplane-ressources : standard bus, user defined bus, ...)
  - **use a standard** that saves investment over longer time scale
  - **use a standard** to have the option to buy commercial available products
    (CPU’s, DAQ components, piggy pack, e.g. IP modules, ...)
  - **use a standard** that offers the option of additional boardspace
    (rear transition option)

Implementation Details

**DESY decision: Use a VME64x system**

- VME64x introduces 5 row (160 pins) connectors J1/J2 and an optional 95pin-connector J0

<table>
<thead>
<tr>
<th>415 pins Total</th>
<th>210 pins VME System</th>
<th>+ 205 pins User Defined</th>
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=> enough pin resources per slot and per backplane to build a compact interlock/control system

- VME is a stable, fast enough and easy to implement bus and instrumentation system
- mixed use of VME and VME64x devices possible
- rear transition board option
- easy system integration

**DESY:** 205 pins User Defined:

- 64 pins per slot used for rear transition
- 141 pins across the backplane to implement a fast user bus
**DESY-VME64x-Backplane**

(slot-pin configuration)

- **J1**: 32 pins per Slot
- **J0**: 19 pins per Slot
- **J2**: 32 pins per Slot

**Interlock / Control Crate**

- **VME-CPU (VME-Controller)**
- **Profibus**
- **Interlock Master / Sequencer**
- **HD**
- **Reserve**

**Up to 16 I/O-Modules**

**Notes:**
- 114 pin User Defined Bus (GTL)
- Rear I/O Connections: 64 pins
- VME64x Standard

1/29/2007  Holger Leich, DESY Zeuthen
Interlock / Control Crate (Side view)

Front Boards (160 mm)
- VMEbus Interface
- Interlock / Master Logic
- I/O resources
- User Bus Interface

Rear Boards (160 mm)
- Rear Transition Signals
- Additional I/O-functions
- Signal conditioning

VME64x Backplane, 160pin-J1/J2, 95pin-J0 (with J0 full & J2-pins rows z,d bussed)

Structure of the DESY User Defined Bus System

Master / Sequencer
- 110 lines connected:
  - 22 Time-Mux-Bus
  - 34 Control-Bus
  - 16 Event-Bus
  - 2 BusInit, BusClock
  - 4 Reserve BusControl
  - 32 Reserve (bi-directional)
  - (all lines GTL)

I/O-Module & other Modules

Event-Bus and/or Reserve could be defined as “LAM” (Emergency Line) for Interlock Signals with very high priority

J1 lines spare at backplane for free use by other (future) components / systems
Bus Timing

• **Time Mux Bus**
  - BCLK
  - Init_l
  - ADDR
  - Data

• **Control Bus**
  - BCLK
  - STRB_l
  - WE_l
  - Address
  - Data

• **Event Bus**
  - BCLK
  - SRVRQ_l

Architecture of the Interlock Master / Sequencer

- EP1K100 FC484
- Ctrl Out
- Ctrl In
- Interlock Logic (Sequencer/Controller)
- Data Out
- Data In
- VME Access Control
- ROM Access Arbiter & Address Mux
- ROM 512 x 16
- DPM Access Control
- Address
- Data
- Data Out
- Data In
- Nonvolatile SRAM 64K x 16
  (4 x U384D256SCSI25)
- VME Bus
- VME Access Control
- VME Interrupt Control
- Control Bus
- Address Bus
- Data Bus
- Bus Timing
- Event Bus
- Time Mux Bus
- Interlock Logic
- EP1K100 FC484
- Ctrl Out
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- Interlock Logic (Sequencer/Controller)
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- VME Access Control
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- Nonvolatile SRAM 64K x 16
  (4 x U384D256SCSI25)
Other Modules under Construction

• Digital Input Module
• Digital Output normal
• Digital Output ultrafast
• Analog IO fast
• Digital IO LWL (Rear Module)

Status of the Project

• Architecture definition ➔ finished
• Backplane design & manufacturing ➔ finished
• Master/Sequencer design ➔ finished/assembled/tested
• I/O Module design ➔ DigiIn: assembled, not yet tested
  DigiOut, DigiOutFast: layout process
  Analog I/O: design not yet finished
  Digital IO LWL: not yet designed
• Firmware design ➔ ongoing
**Existing RF Interlock System**

![Image of RF Interlock System]

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**VME64x-Crate with DESY VME64x Backplane**

![Image of VME64x-Crate]

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Interlock Master / Sequencer Module