CMS Pixel Detector Upgrade

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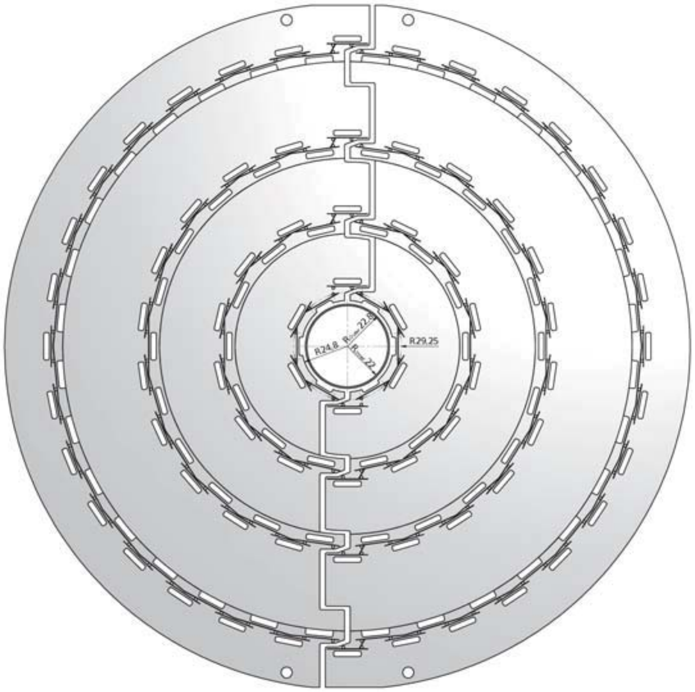
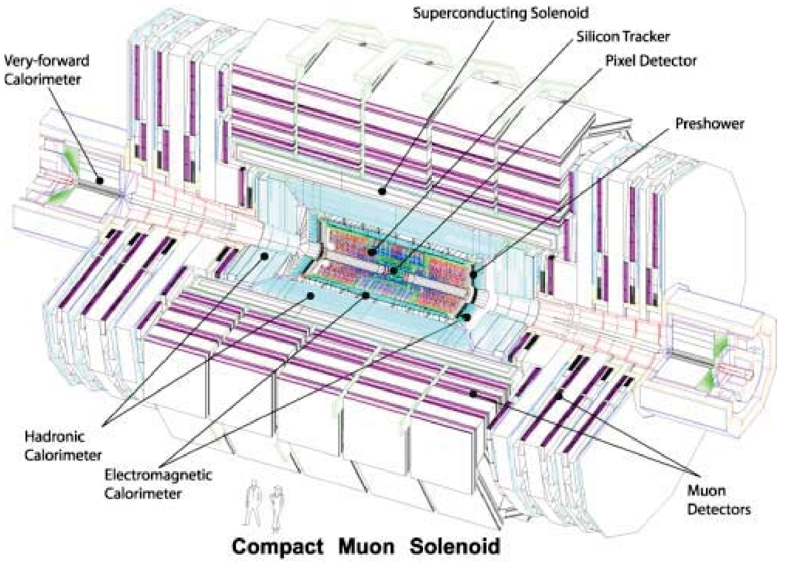
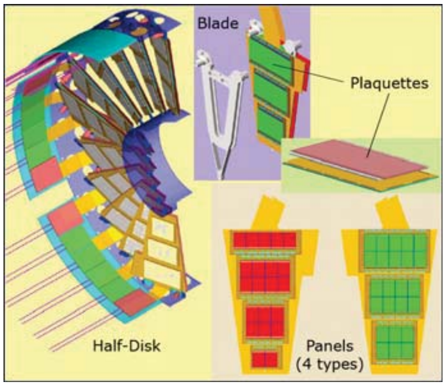
DESY Technisches Seminar 22.11.2011



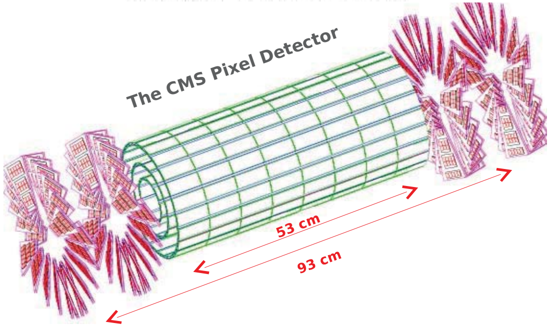
- Present pixel detector
- 4-layer upgrade
- Read out chip modifications
- Module assembly, testing, and calibration
- preparations at DESY and Uni Hamburg

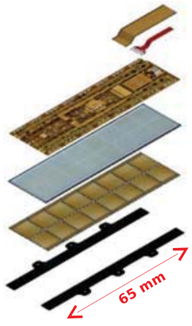
CMS and its pixel detectors





Panels of the Forward Pixel Detector



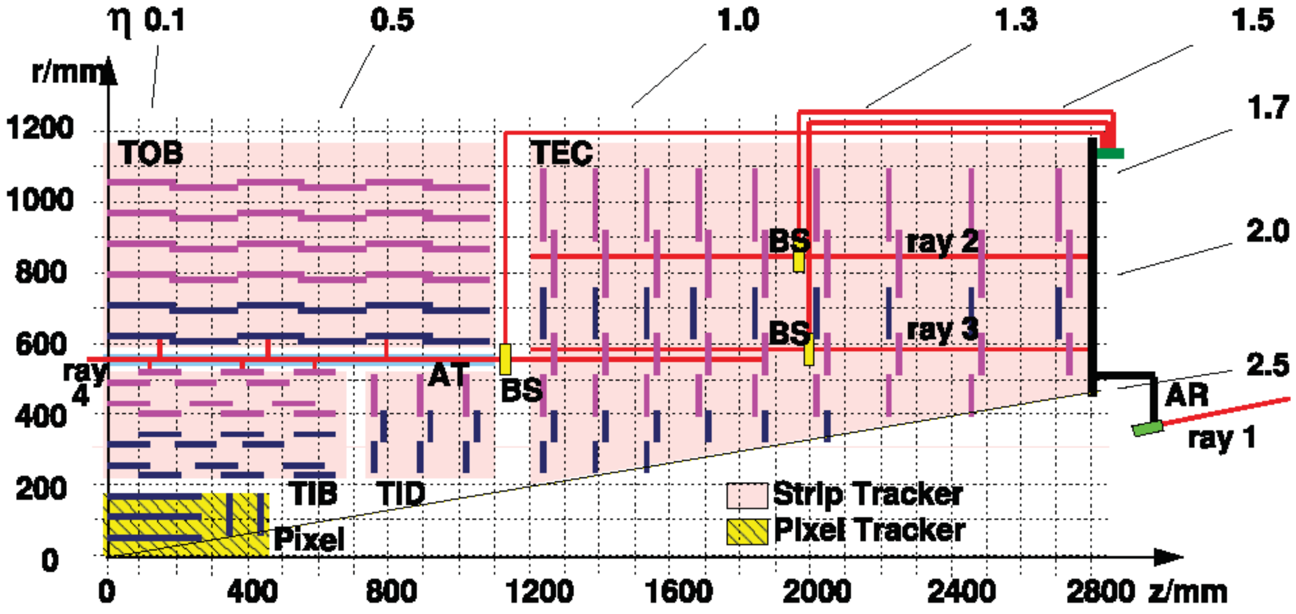


Forward Pixel Detector has 2 disks on each side at z = 34.5 cm and 46.5 cm.
FPix has 672 modules.

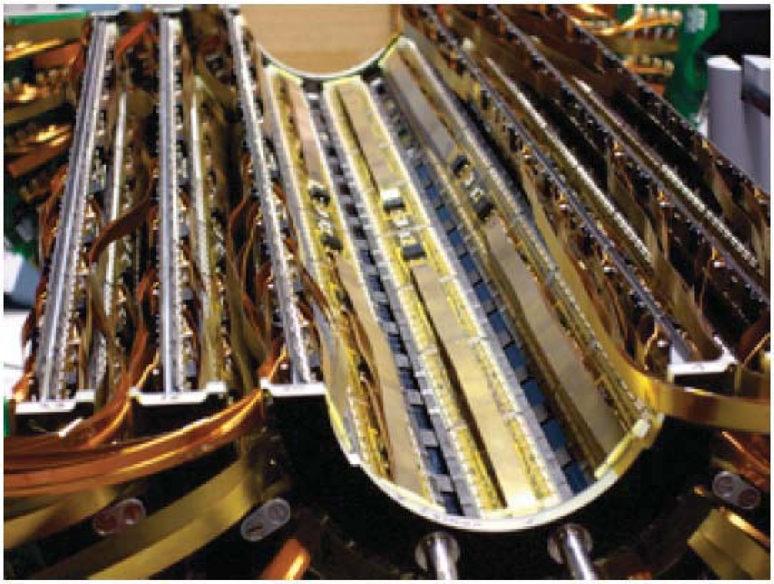
Barrel Pixel Detector has 3 layers at R = 4.4 cm, 7.3 cm, and 10.2 cm.
BPix has 768 modules.

Total of ~15,840 readout chips, 66M pixels.

CMS Si Tracker

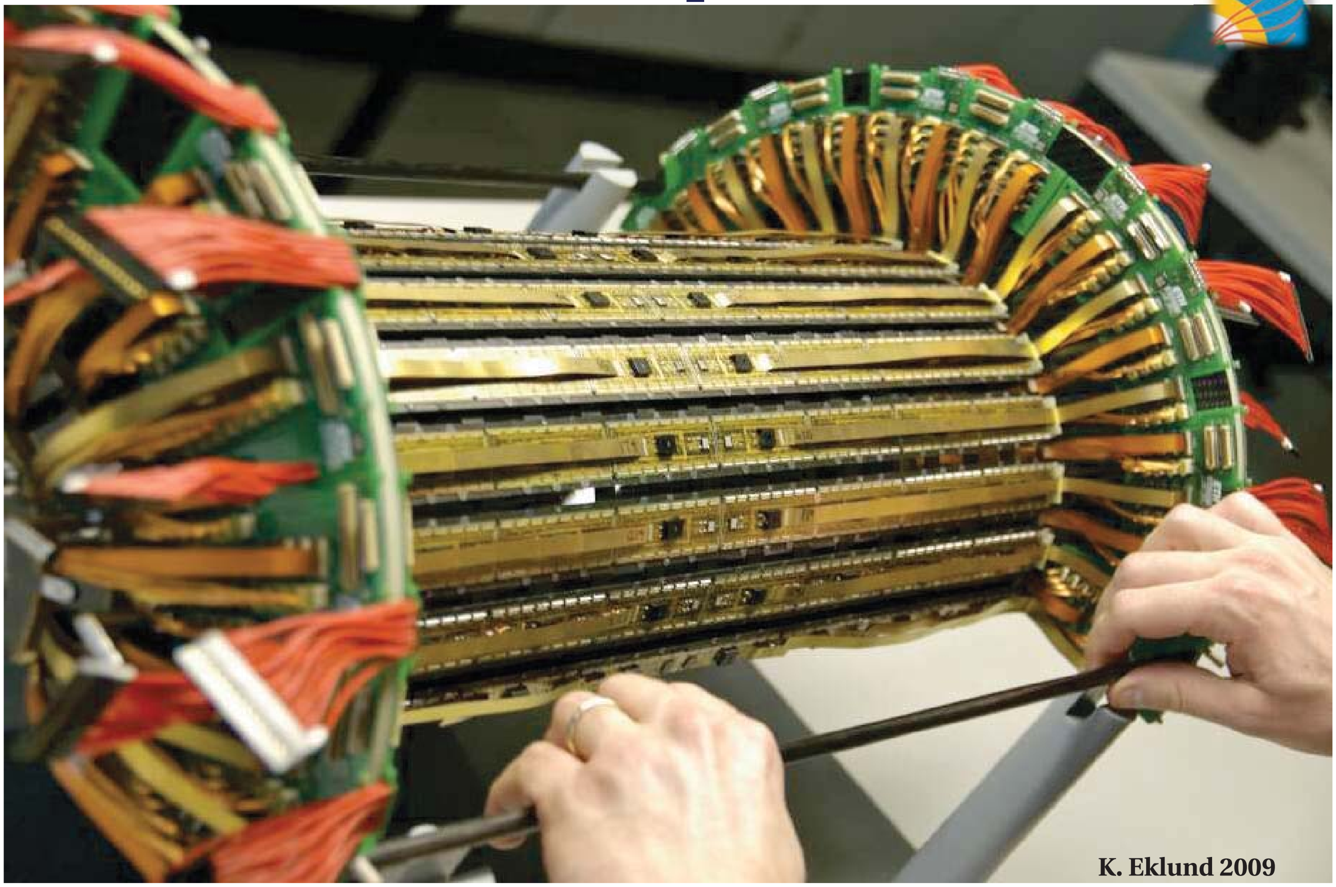


CMS at present: 3 barrel pixel layers



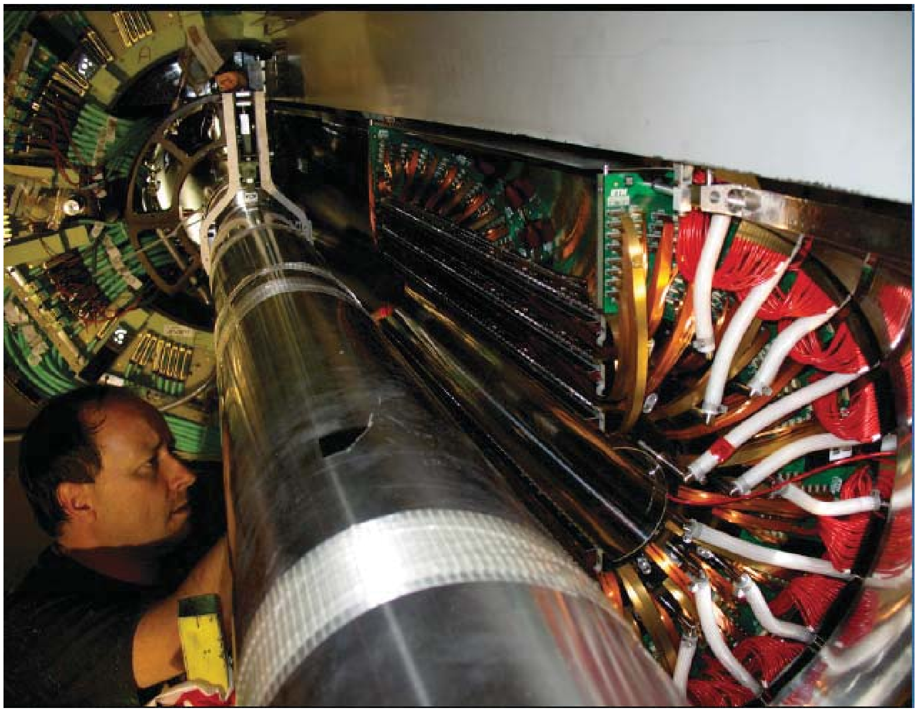
- Developed and built at PSI, CH, 1994 - 2008.
- Active length 52 cm.
- 3 layers:
  - <R> = 4.4, 7.3, 10.2 cm
- 768 modules
- 12'000 chips
- 51M pixels
- 1.5 kW
- 5.2 kg

Present barrel pixel detector



K. Eklund 2009

Barrel Pixel insertion 2008



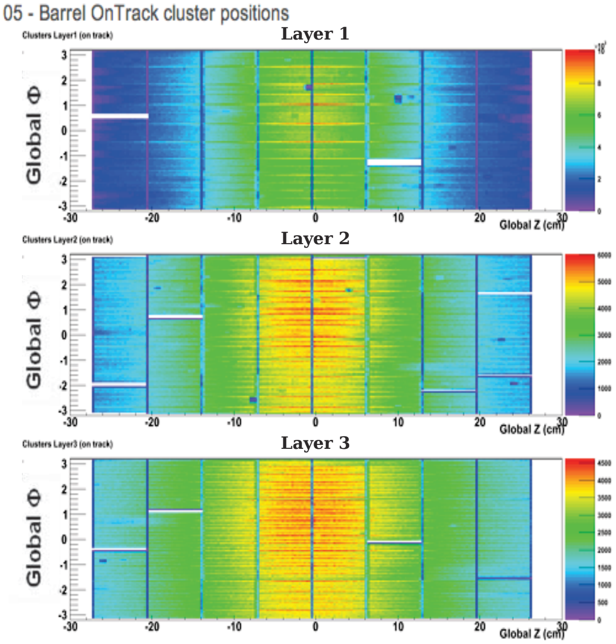
- The CMS pixel detector is accessible and removable during extended Christmas maintenance.
- Removal required for beam pipe bake out (vacuum conditioning).
- There is space for a 4th barrel layer.

Conical beam pipe: smaller at the IP.

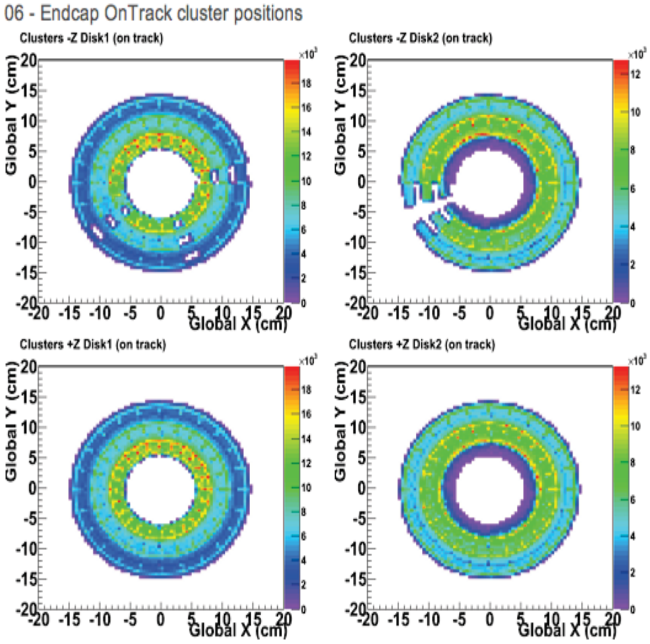
Pixel operation in 2010

- 98.7% alive barrel modules.
- 96.4% alive forward modules.

05 - Barrel OnTrack cluster positions

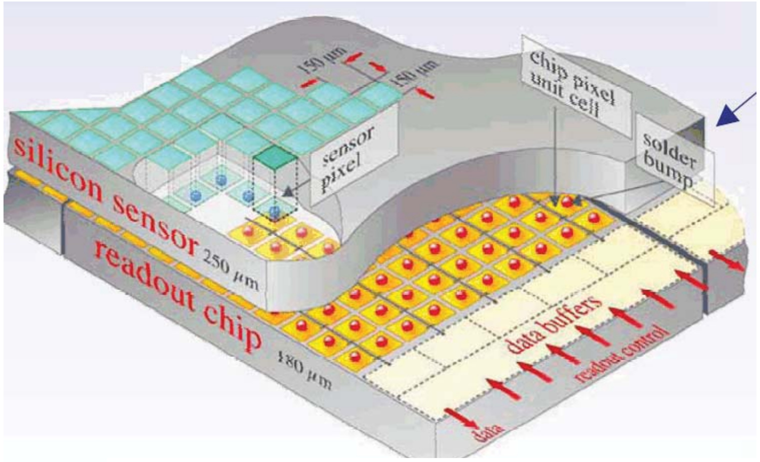


06 - Endcap OnTrack cluster positions



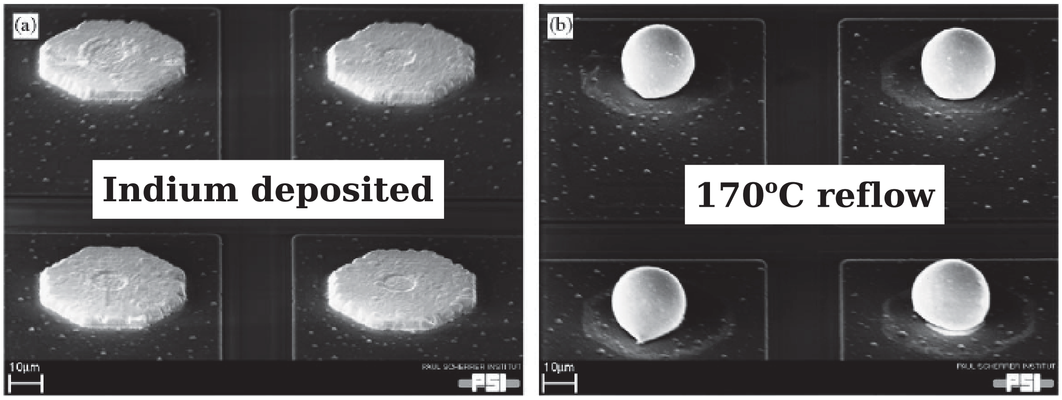
status Aug 2010

Hybrid pixel detectors



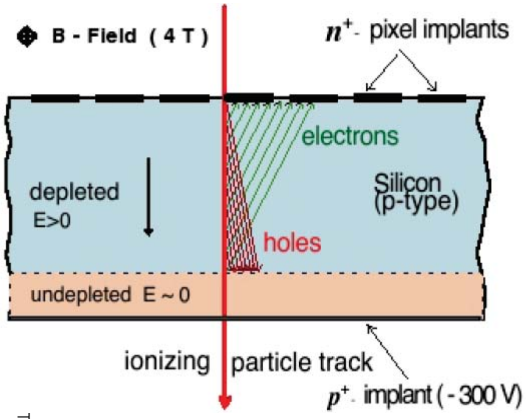
Silicon sensors with $100 \times 150\ \mu m^2$ pixels, bump bonded to CMOS readout chips.

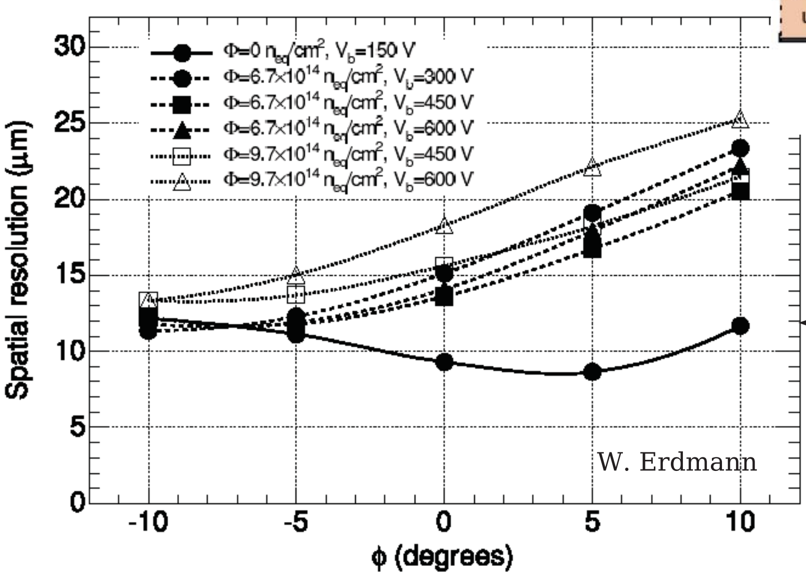
Requires special bump bond technology.
Cost driver: 2c/bump.



CMS Pixel hit resolution

Drift in crossed E and B fields:
Lorentz angle ($\tan \alpha_L = \mu B$) is
~28° for e in pure Si at 3.8 T.
Leads to beneficial charge sharing.

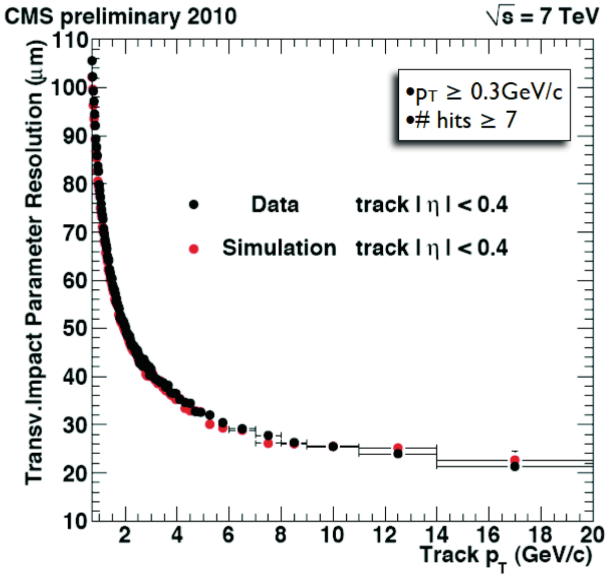


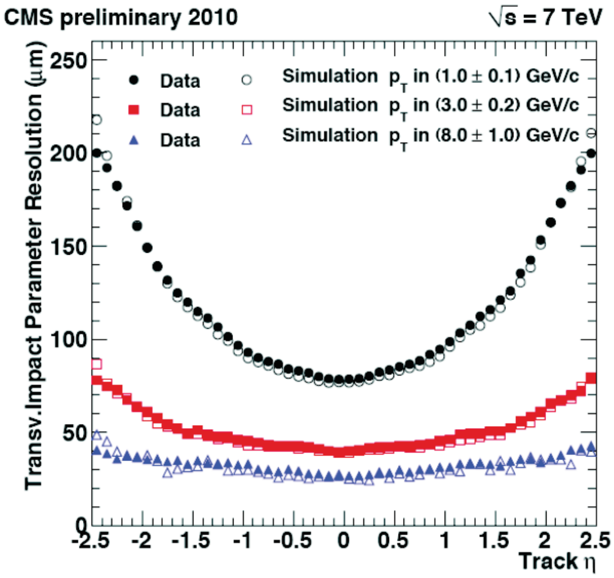


W. Erdmann

a hit resolution of 12 µm has been achieved in 2010 collision data.

CMS track impact parameter resolution

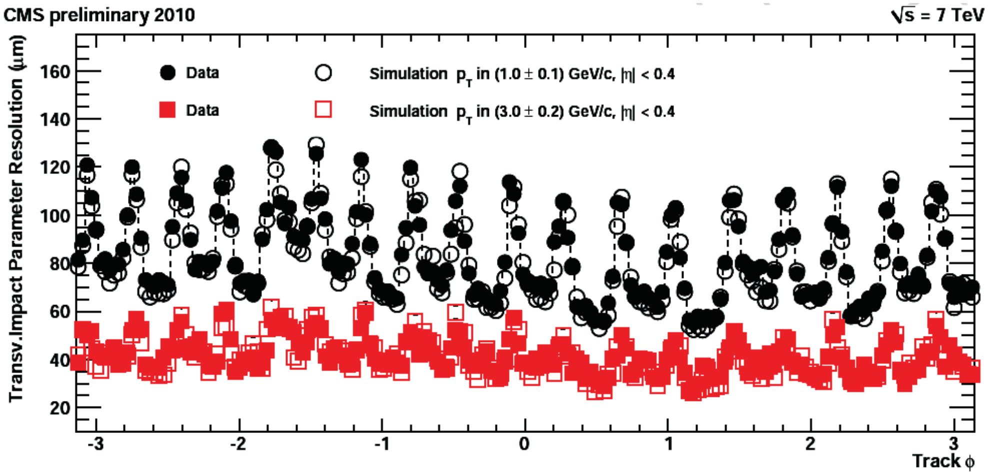




Reach 20 µm
at high momentum.
Ultimately expect 12 µm.

Limited by multiple scattering at low momenta and/or high rapidity.

CMS impact parameter resolution

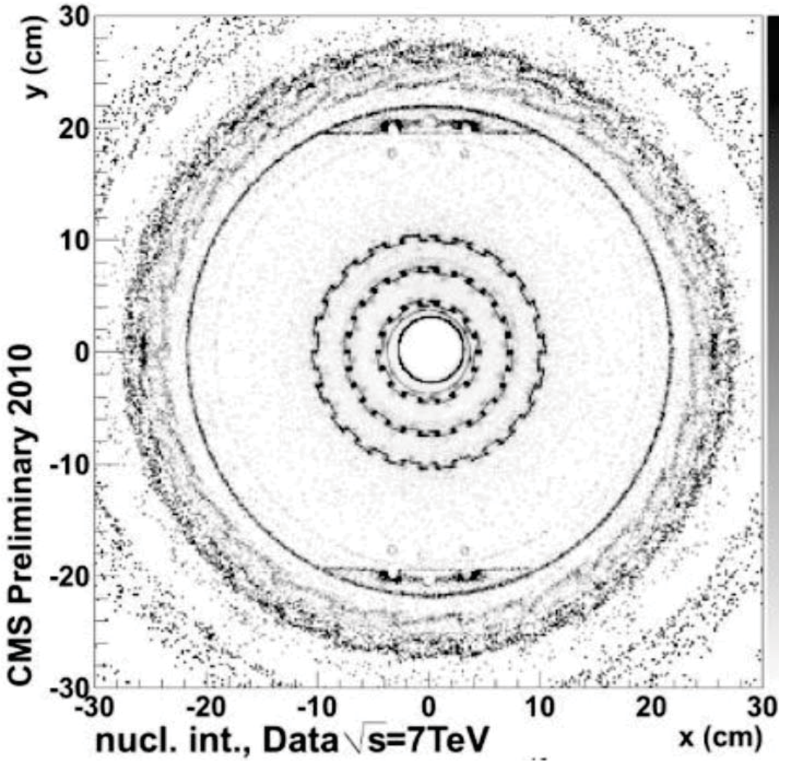


1 GeV

3 GeV

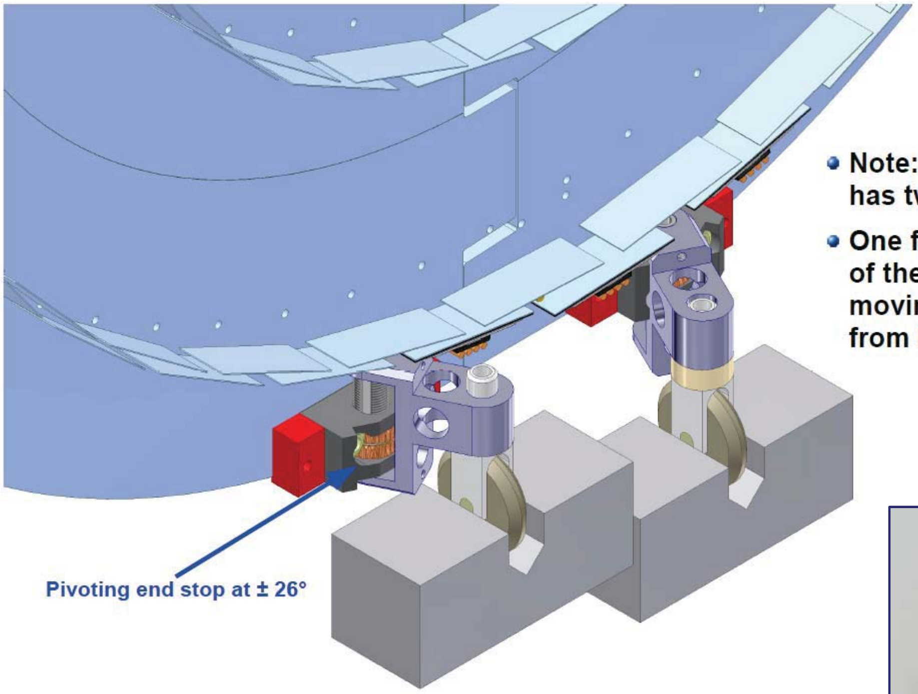
- 18-fold ϕ structure due to pixel cooling pipes visible at low p_T.
- Well described by the detector simulation.

Nuclear imaging

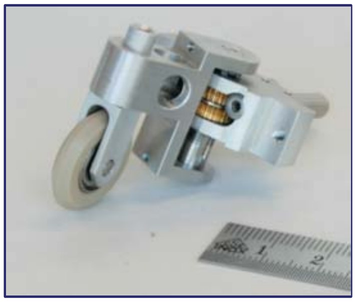


- Reconstructed nuclear interaction vertices.
  - Barrel pixel region.
- CMS tracker is shifted by ~3 mm relative to the machine beam pipe.
  - Upgrade: center pixel around pipe!
- Pixel modules, cooling pipes and support rails visible.
  - Upgrade: reduce the material budget!

CMS Barrel pixel adjustable wheels

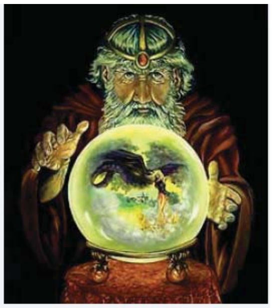


- Note: Lower wheel set has two worm gears.
- One for lifting/lowering of the BPIX and one for moving towards/away from beam pipe



Mechanical mock-up will be prepared.
Test installation procedure in early 2014.

LHC plan (S. Bertolucci PLHC 2011)



2009 — Start of LHC

Run 1: 7 TeV centre of mass energy, luminosity ramping up to few 10^{33} cm^{-2} s^{-1}, few fb^{-1} delivered

2013/14 — LHC shut-down to prepare machine for design energy and nominal luminosity

Run 2: Ramp up luminosity to nominal (10^{34} cm^{-2} s^{-1}), ~50 to 100 fb^{-1}

2017 or 18 — Injector and LHC Phase-I upgrades to go to ultimate luminosity

Run 3: Ramp up luminosity to 2.2 x nominal, reaching ~100 fb^{-1} / year accumulate few hundred fb^{-1}

~2021/22 — Phase-II: High-luminosity LHC. New focussing magnets and CRAB cavities for very high luminosity with levelling

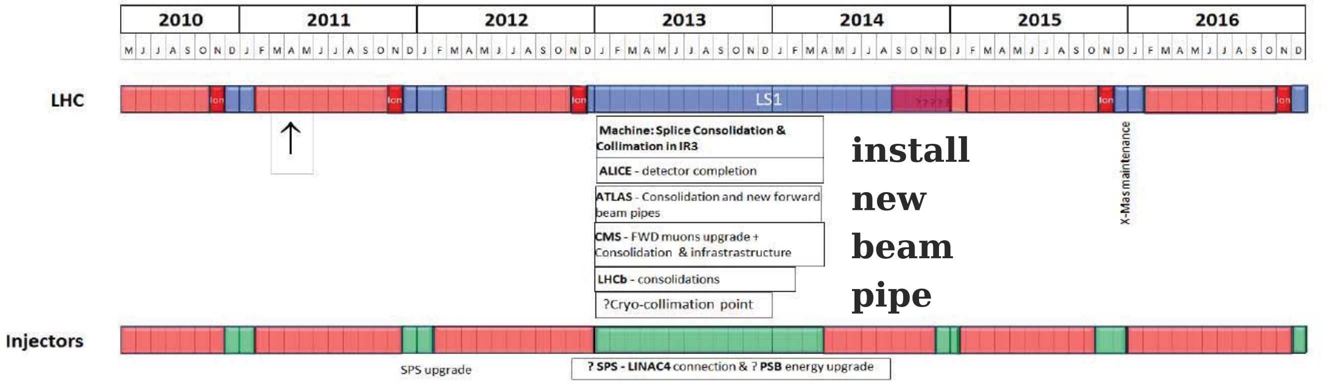
Run 4: Collect data until > 3000 fb^{-1}

2030 — ILC, High energy LHC, ... ?

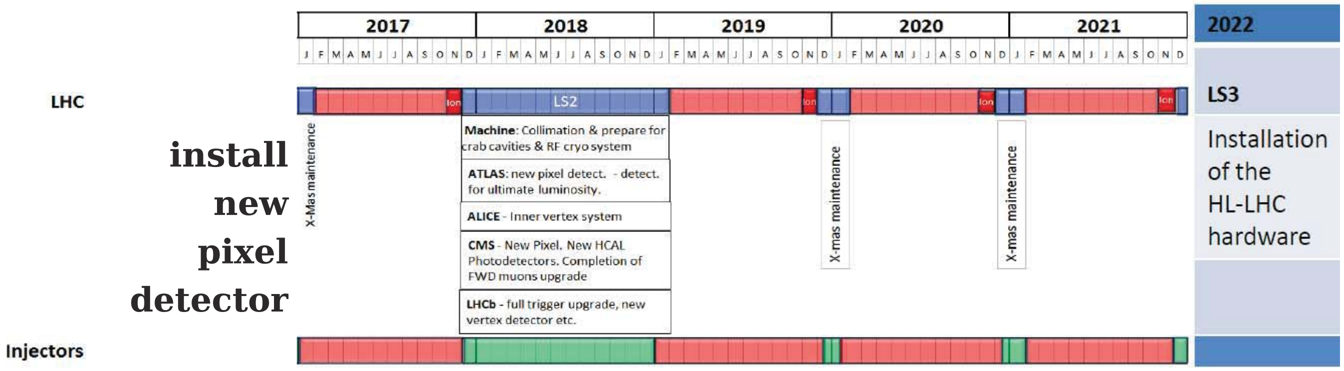
pixel upgrade needed

new tracker needed

LHC 10 year plan as of June 2011



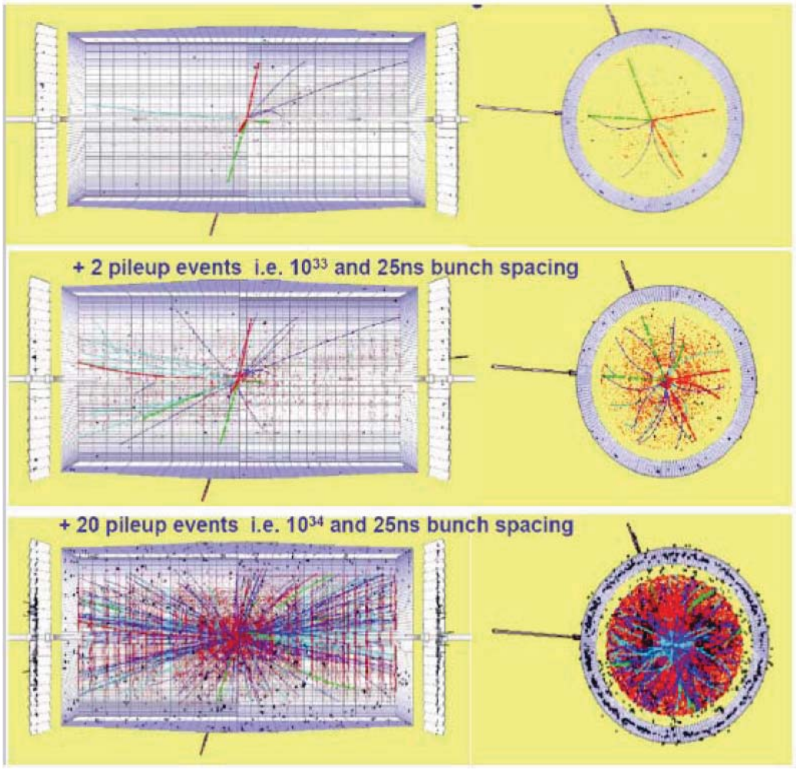
install
new
beam
pipe



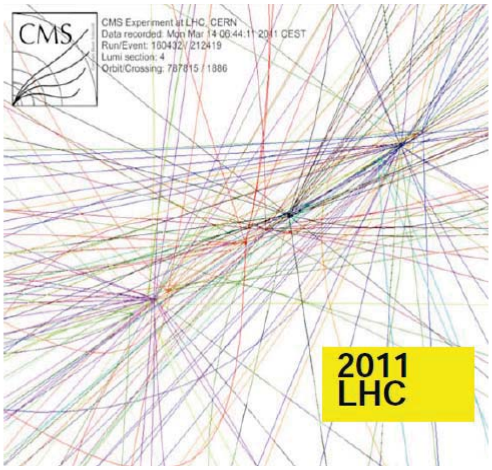
install
new
pixel
detector

Event pile-up at high luminosity

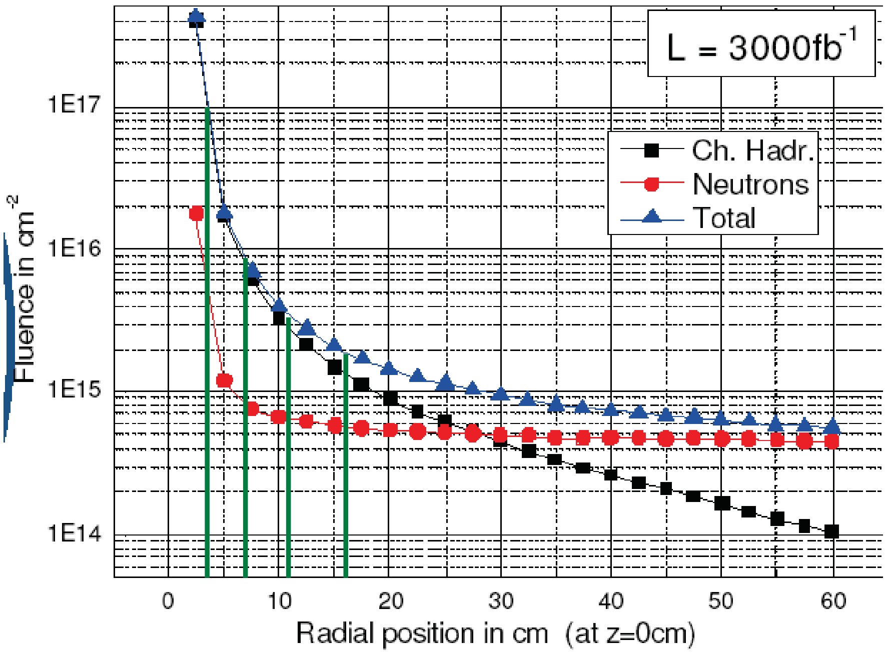
Simulation



Data 2011:
7 pile-up events
at $2 \cdot 10^{33}$ and 50 ns
bunch spacing



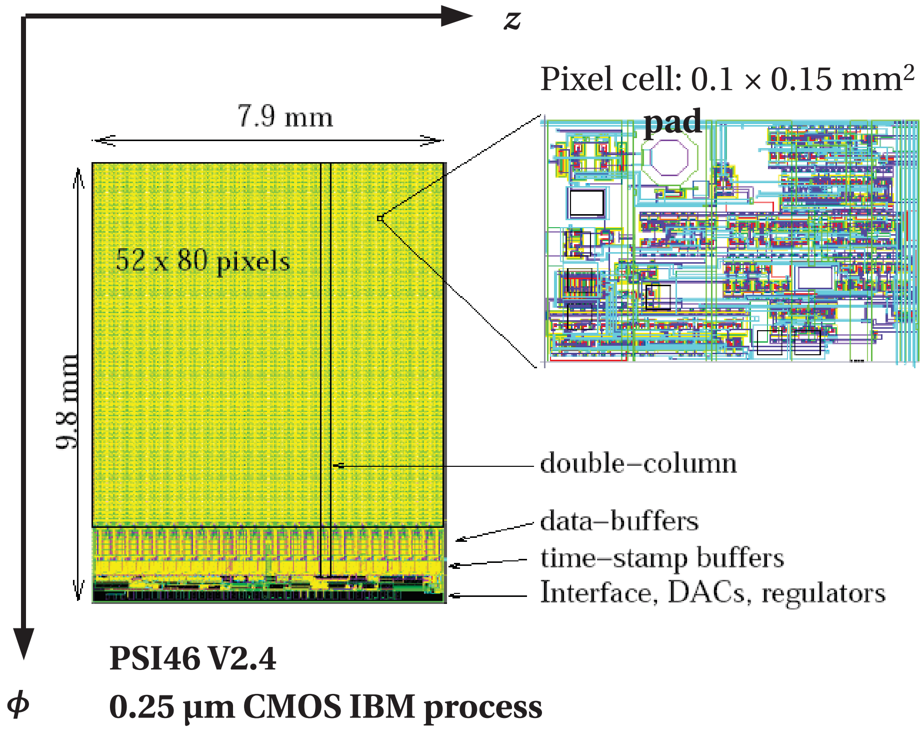
Particle fluence



- 3000 fb^{-1} = 20 years.
- This decade: 300 fb^{-1}.
- Pixel region: dominated by pions.
- Layer at R = 3 cm:
  - flux 500 MHz/cm^2,
  - may need replacement every year (200 fb^{-1}).

F. Hartmann, sensor testing, CMS Tracker Week Sep 2009
http://indico.cern.ch/conferenceDisplay.py?confId=47301

CMS Pixel Chip



Pixel cell: 0.1 × 0.15 mm^2

double–column

data–buffers

time–stamp buffers

Interface, DACs, regulators

noise 130 e

V_A = 1.5 V

V_D = 2.5 V

30 μW / pixel

0.12 W / chip

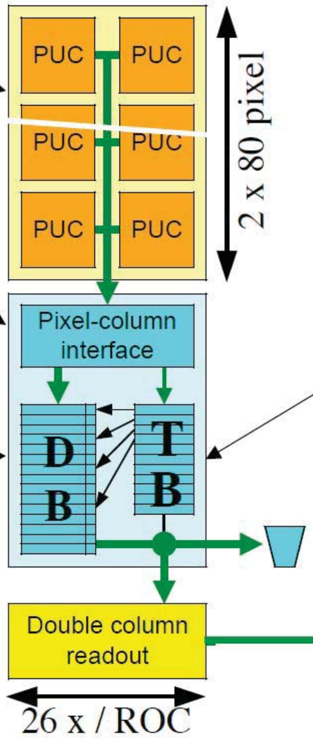
PSI46 V2.4
0.25 μm CMOS IBM process
radiation hard design
1.3 M transistors

operational after 130 kGy γ irradiation

Double column readout

Sources of inefficiency:

now → upgrade



Pixel busy:
pixel insensitive until hit transferred to data buffer (column drain mechanism)

2BC → 1BC

Double column busy:
Column drain finds hitted pixels and transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted

3 → 8 pending

Data Buffer full:
size: **80** (32)

Double column:
2×80 pixel, 0.024 cm^2
L1 trigger:
after 3.2 us (130 BC).

at 2 10^{34}, 25 ns, 29 mm:
0.2 tracks / DC / BC,
25 tracks in buffers.

Timestamp Buffer full:
size: **24** (12)

Readout and double column reset:
Wait for token, reset after r/o

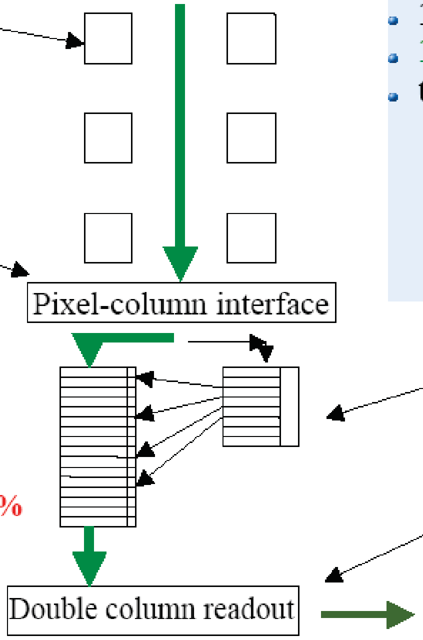
40 MHz analog readout
→ 160 MHz digital

Data loss mechanisms

Present PSI46 readout chip simulated at LHC design luminosity

Pythia physics generator + detector and chip simulation:

- 1xLHC: 10^{34}cm^{-2}s^{-1}
- 11 cm / 7 cm / 4 cm layer
- total data loss @ 100kHz L1A:
  - 0.8%
  - 1.2%
  - 3.8%



Pixel busy:
0.04% / 0.08% / 0.21%
pixel insensitiv until hit transferred to data buffer (column drain mechanism)

Double column busy:
0.004% / 0.02% / 0.25%
Column drain transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted

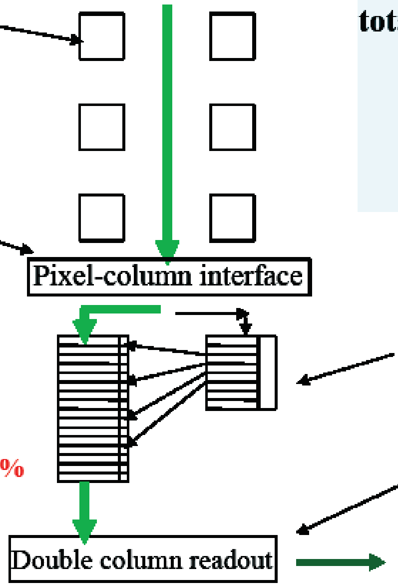
Data Buffer full:
0.07% / 0.08% / 0.17%

Timestamp Buffer full:
0 / 0.001% / 0.17%

Readout and double column reset:
0.7% / 1% / 3.0%
for 100kHz L1 trigger rate

Data loss mechanisms

Present PSI46 readout chip simulated at 2× LHC design luminosity



Pixel busy:
0.09% / 0.18% / 0.48%

Double column busy:
0.003% / 0.18% / 1.3%

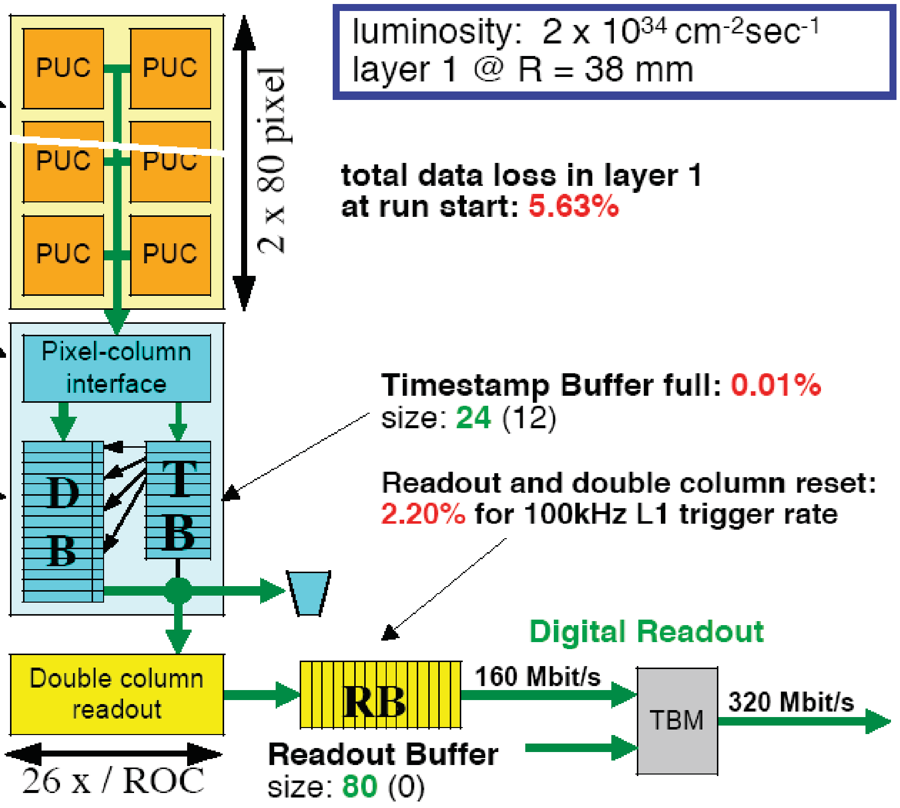
Data Buffer full:
0.09% / 0.17% / 0.83%

Timestamp Buffer full:
0 / 0.05% / 6.8%

Readout and double column reset:
1.1% / 2.1% / 6.7%
for 100kHz L1 trigger rate

total data loss @ 100kHz L1A:
1.3% @ 11cm
2.7% @ 7cm
16% @ 4cm

Data loss with extended buffering



luminosity: 2 x 10^{34} cm^{-2}sec^{-1}
layer 1 @ R = 38 mm

total data loss in layer 1 at run start: 5.63%

Pixel busy: 0.72%
pixel insensitive until hit transferred to data buffer (column drain mechanism)

Double column busy: 2.03%
Column drain finds hitted pixels and transfers hits from pixel to data buffer. Maximum 3 pending column drains requests accepted

Data Buffer full: 0.68%
size: 80 (32)

Timestamp Buffer full: 0.01%
size: 24 (12)

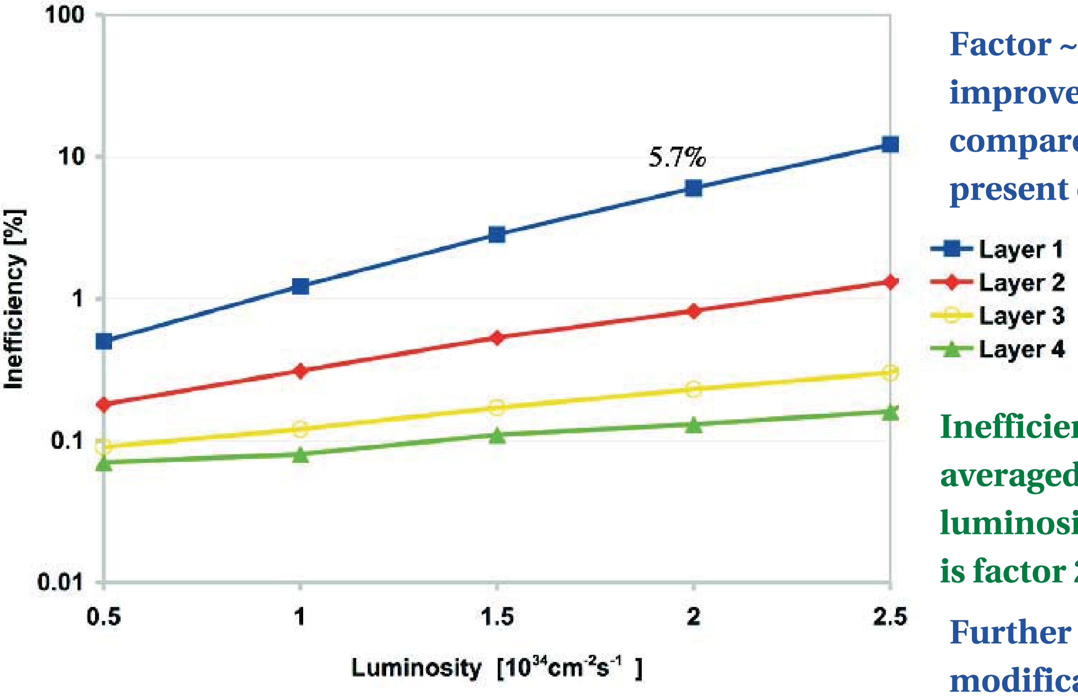
Readout and double column reset:
2.20% for 100kHz L1 trigger rate

Readout Buffer
size: 80 (0)

H.C. Kaestli
Oct 2009

Data loss vs luminosity

Pixel readout chip simulation with increased buffering



at 4 cm

H.C. Kaestli
Oct 2009

Factor ~3 improvement compared to the present chip.

Inefficiency averaged over a luminosity fill is factor 2 smaller.

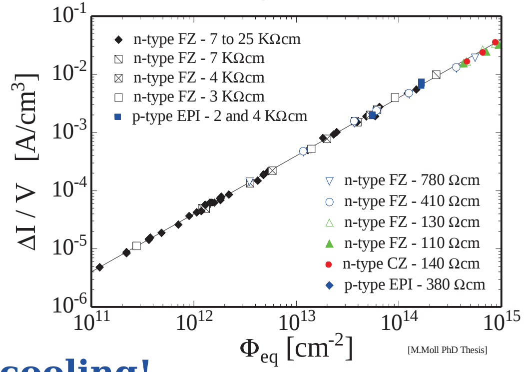
Further design modifications under study: aim for 2.5% at 2 10^{34}

Radiation damage in silicon

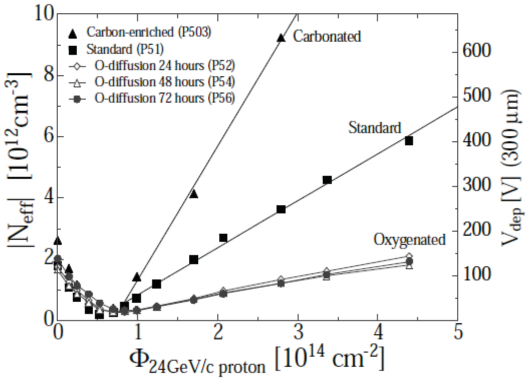
- Leakage current:
  - I / Vol = α Φ (fluence Φ [particles/cm2])
  - all silicon materials (FZ, Cz, epi) have the same damage α.
  - only cooling helps to reduce leakage current (factor 2 / 8°C).
- Space charge creation ('type inversion'):
  - leads to high depletion voltage at high fluence.
  - oxygenated silicon is better (DOFZ, mCz).
  - cooling reduces activation of defects.
- Charge trapping:
  - reduces charge collection efficiency
  - collecting electrons (n-in-p or n-in-n) is better than holes (p-in-n).
  - no 'defect engineering' method known to help.
  - Charge amplification at high bias, earlier in thin sensors or 3D.

Radiation damage effects in silicon

leakage current

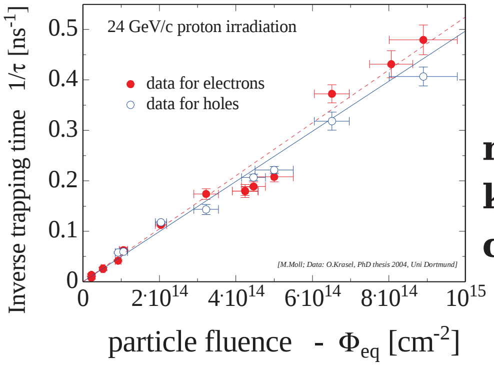


depletion voltage



cooling!
factor 1/2
every -8°C

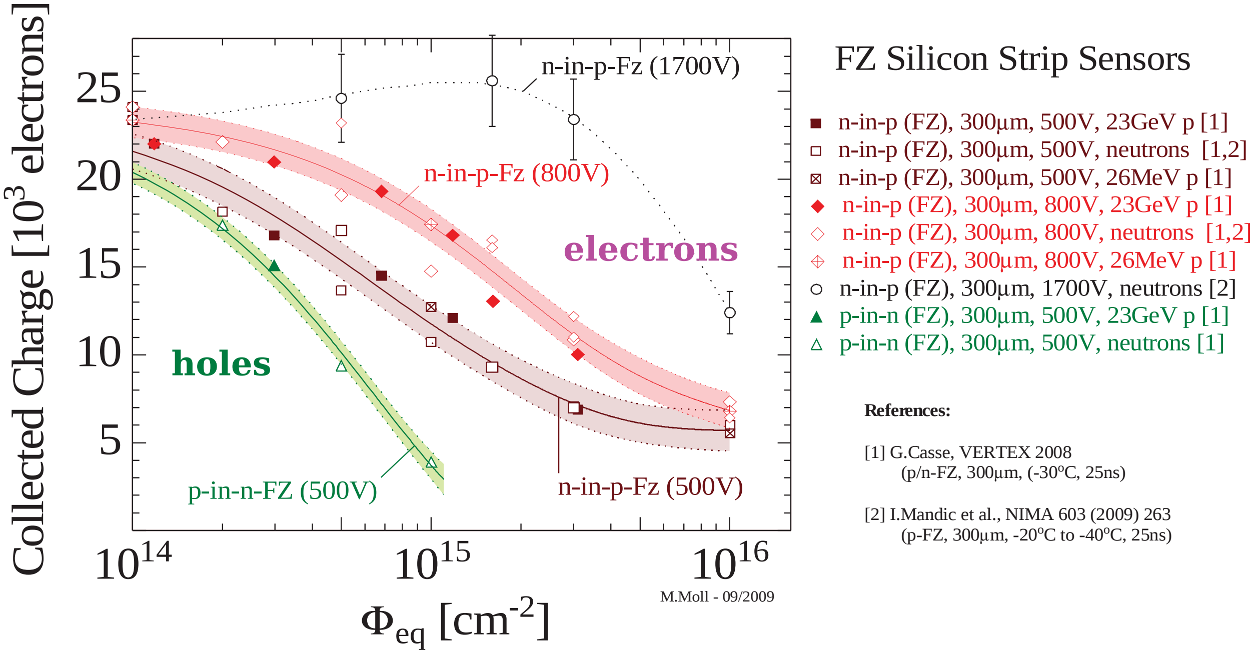
trapping



no
known
cure

oxygenated
Si used!
Keep Si cool
to avoid
activation
of defects.

Silicon charge collection vs fluence



References:

[1] G.Casse, VERTEX 2008
(p/n-FZ, 300µm, (-30°C, 25ns)

[2] I.Mandic et al., NIMA 603 (2009) 263
(p-FZ, 300µm, -20°C to -40°C, 25ns)

Detectors made from oxygenated Si and collecting electrons should operate up to a few 10^{15} n_{eq}/cm^2 with tolerable efficiency and resolution degradation: that's several 100 fb^{-1} at R = 3 cm.

Further upgrade considerations

- Smaller beam pipe for improved impact parameter resolution:
  - B-tagging
- 4th layer for better track seeding efficiency and improved stand-alone tracking:
  - High Level Trigger
- Less material (mechanics, chips, cooling, cables):
  - less multiple scattering, photon conversions, nuclear interactions

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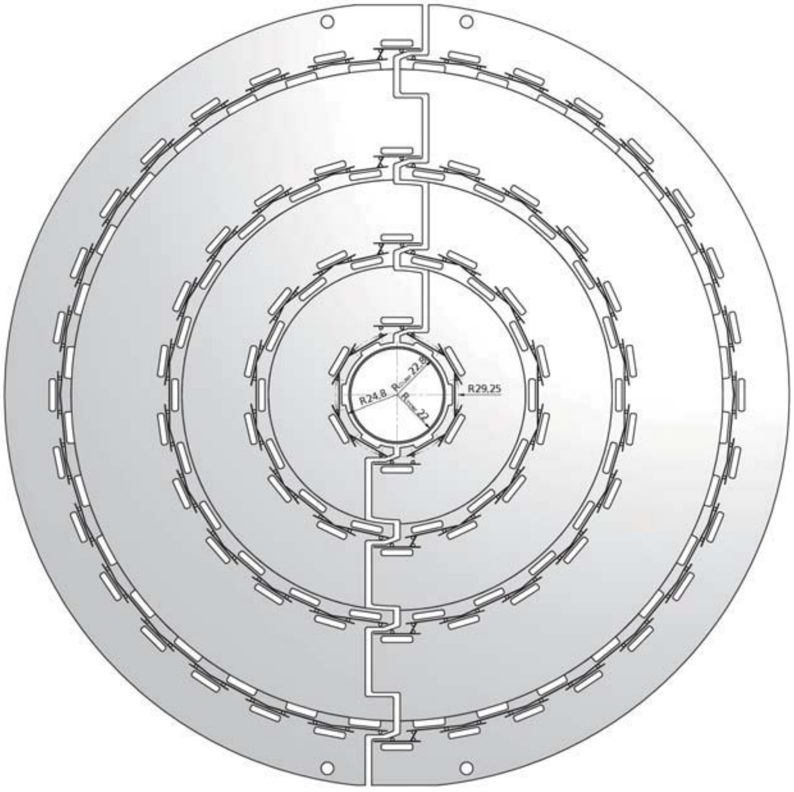
CMS pixel upgrade: 4 layers



2 identical half-shells.
1184 modules (79M pixels)
(1.6 × present barrel)

R_1 = 29 mm, 96 modules

CH

(reduce beam pipe diameter from 59 to 45 mm)

R_2 = 68 mm, 224 modules

CH

R_3 = 109 mm, 352 modules

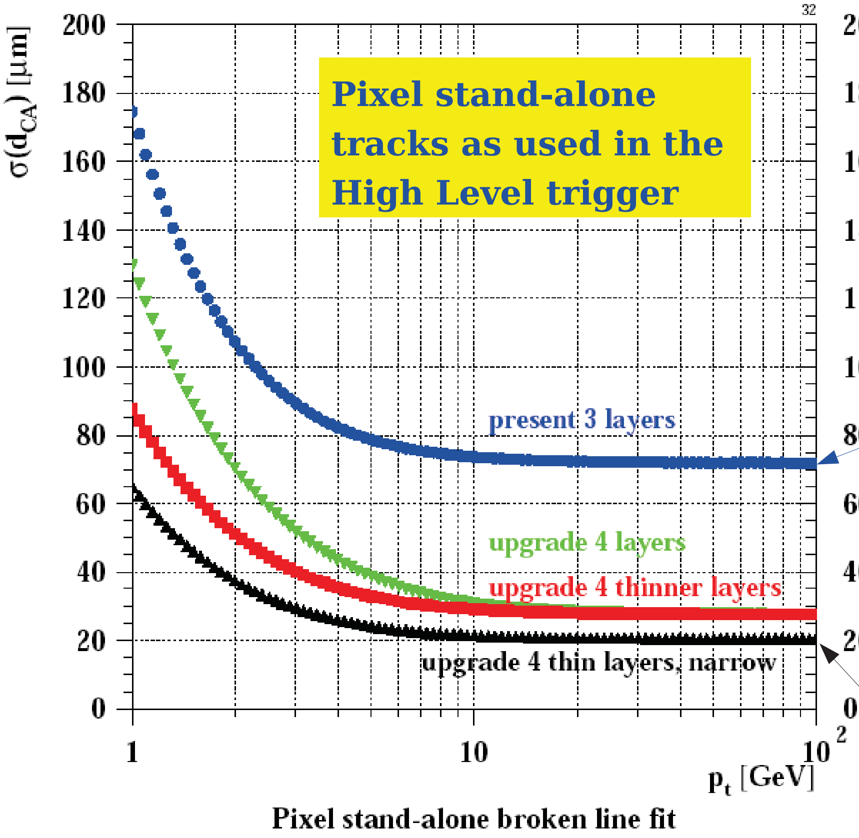
Italy, CERN

R_4 = 160 mm, 512 modules

Germany

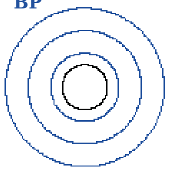
Roland Horisberger, CMS Tracker week Dec 8, 2009
http://indico.cern.ch/conferenceDisplay.py?confId=75797

Pixel track impact parameter resolution



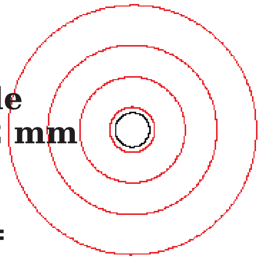
Pixel stand-alone tracks as used in the High Level trigger

present
R_{BP}=29 mm



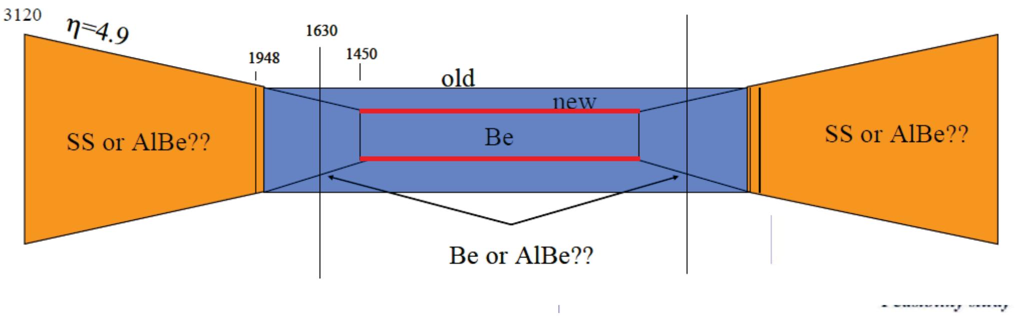
$\sigma(d_{CA})$ =
160 µm / pt ⊕ 72 µm

upgrade
R_{BP}=22 mm



$\sigma(d_{CA})$ =
62 µm / pt ⊕ 20 µm

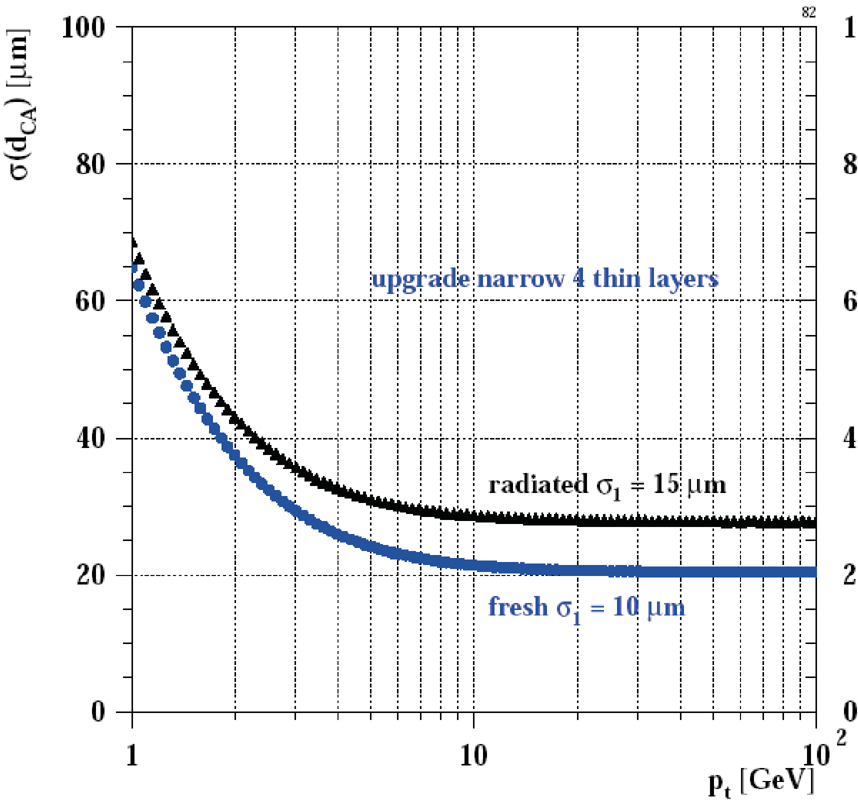
CMS new central beam pipe



new central beam pipe with
43.6 mm inner diameter
(present: 58 mm)
accepted by LHC machine.
Order will be placed soon.
Aim to install Jan 2014.

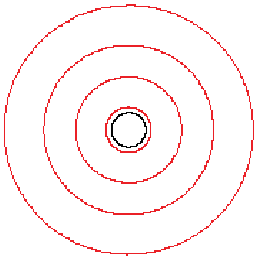
Austin Ball
June 2011

Radiation damage



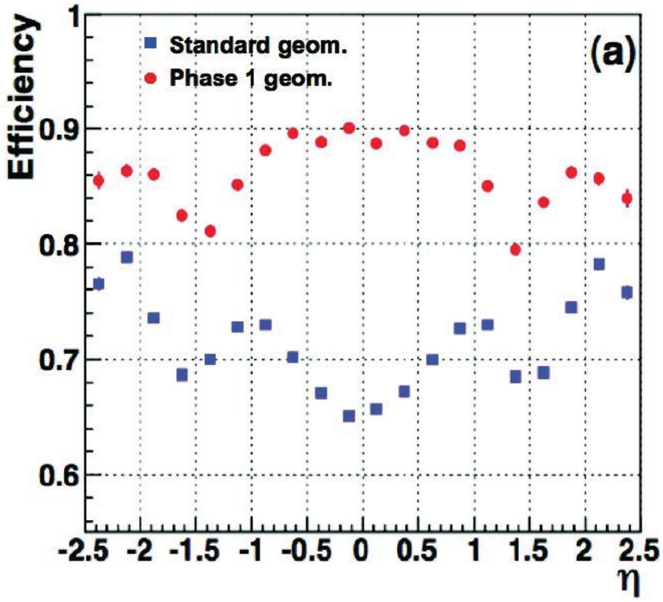
Pixel stand-alone broken line fit

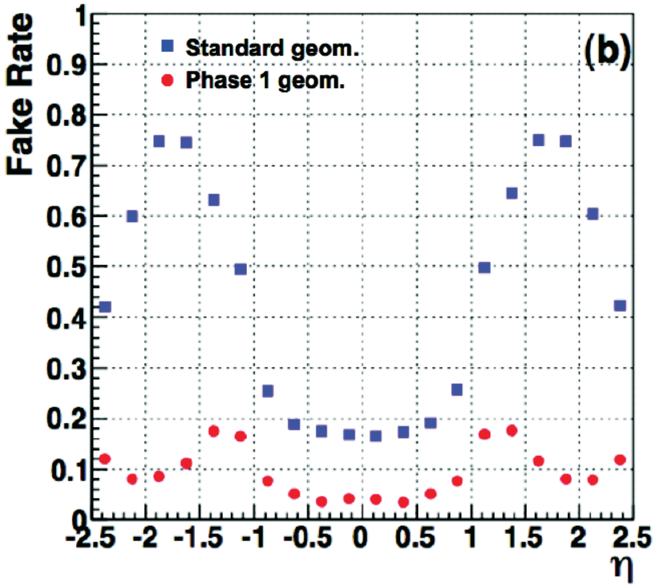
4-layer upgrade
R_{BP} = 22 mm



Tracking performance with pile-up 50

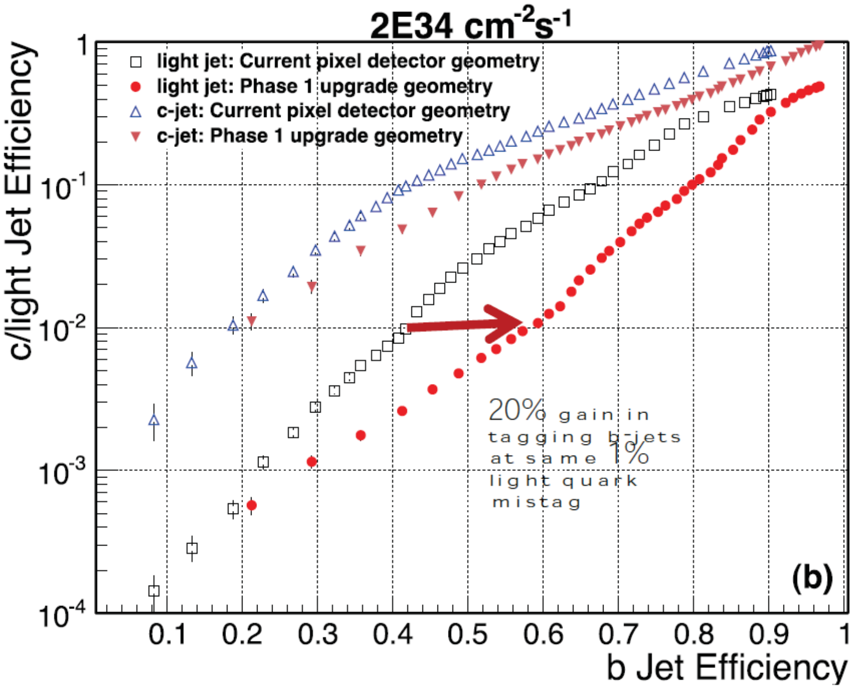
- t-tbar simulation with pile-up of 50 minimum bias events ($2 \cdot 10^{34}$ with 25 ns spacing).
- Pixel-based track seeding.





- **4-layer upgrade improves seeding efficiency.** z-gaps remain
- **4-layer upgrade reduces fake rate.**

b-tagging performance with pile-up 50



20% gain in tagging b-jets at same 1% light quark mistag

- Detailed simulation of the physics performance on going:
  - at high level trigger,
  - at full analysis level.
- 4-layer upgrade is needed to maintain present performance at high luminosity
  - Expect improved pixel b-tagging in the HLT.

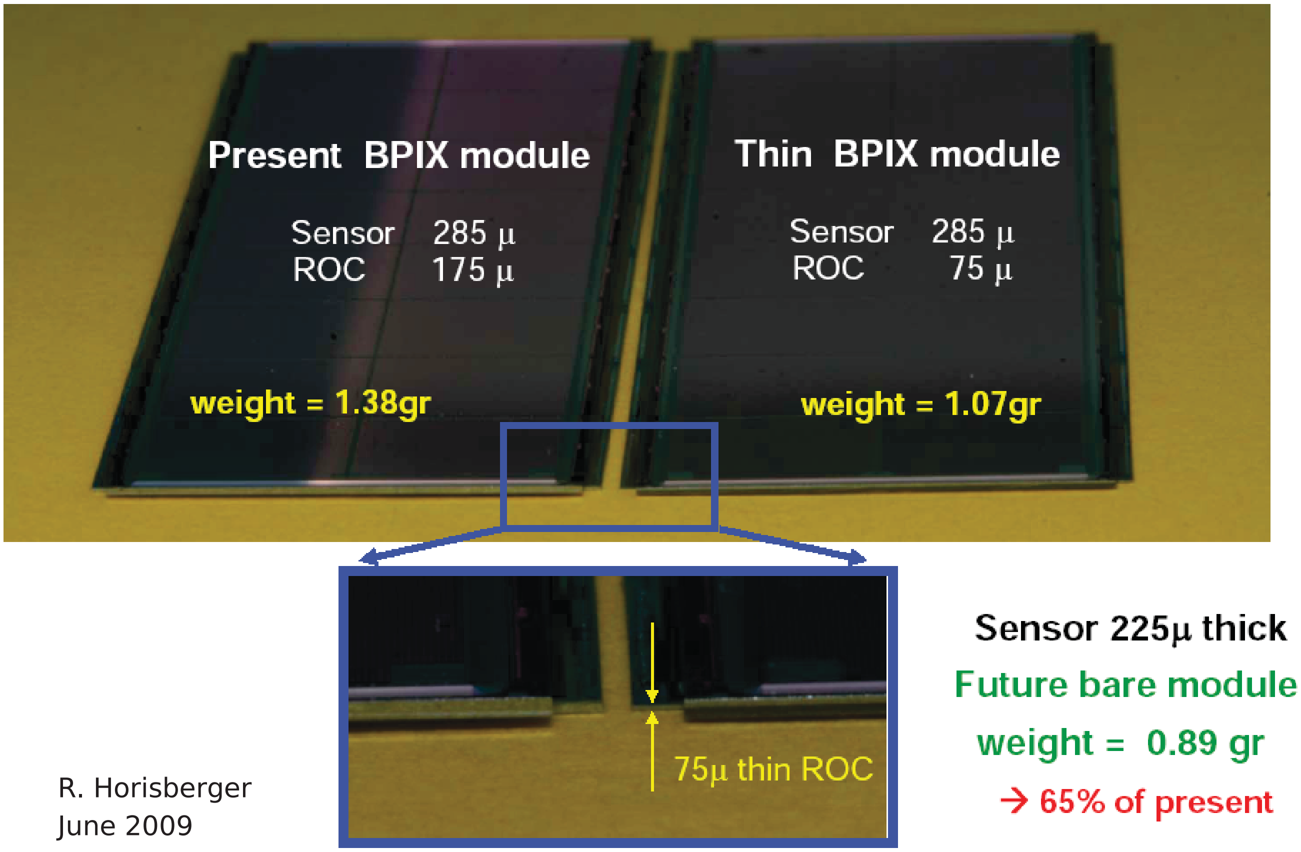
Pixel upgrade motivations

- Prepare for 2× higher luminosity than design: $2 \cdot 10^{34}/\text{cm}^2/\text{s}$:
  - maintain pixel efficiency
- Less material (mechanics, chips, cooling, cables):
  - less multiple scattering, photon conversions, nuclear interactions
- 4th layer for better track seeding efficiency and improved stand-alone tracking:
  - High Level Trigger
- Smaller beam pipe for improved impact parameter resolution:
  - B-tagging
- Add redundancy in the tracking system:
  - independent of the luminosity evolution

Pixel upgrade implications

- Prepare for 2× higher luminosity than design: $2 \cdot 10^{34}/\mathrm{cm}^2/\mathrm{s}$:
  - Requires a new readout chip with more buffering.
- Less material:
  - Low mass supports, CO_2 cooling, optical converters outside the tracking volume.
- 4th layer for better track seeding efficiency and improved stand-alone tracking:
  - Digital readout and DC-DC power converters (have to use the same outer power cables and optical fibers)
- Smaller beam pipe for improved impact parameter resolution:
  - Accepted by LHC machine group.
- Add redundancy in the tracking system:
  - Be ready early, almost independent of the luminosity evolution.

CMS pixel upgrade



Sensor 225µ thick

Future bare module

weight = 0.89 gr

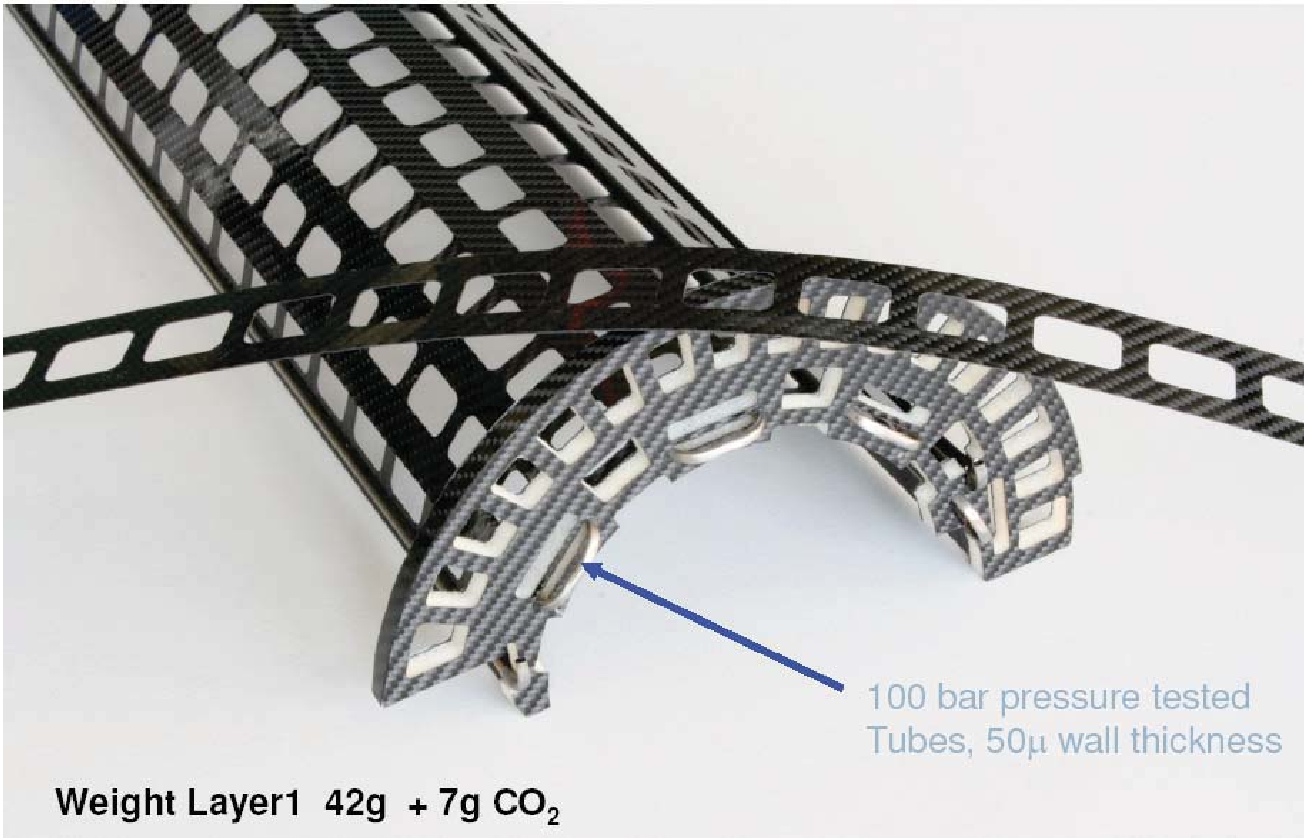
→ 65% of present

R. Horisberger
June 2009

Upgrade carbon fiber frame

Ultra-leight weight carbon fibre frame and airex end flange with pipes for CO2 cooling.

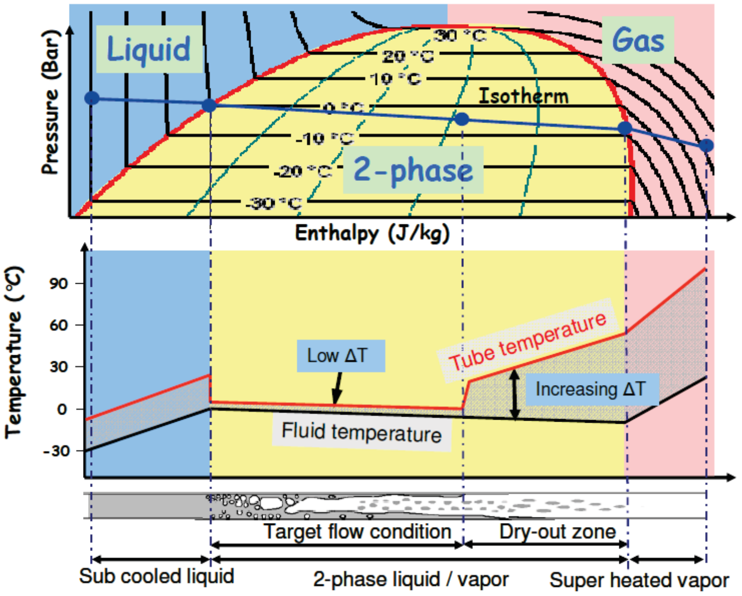
CMS pixel upgrade

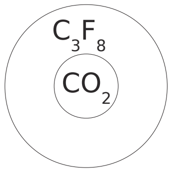


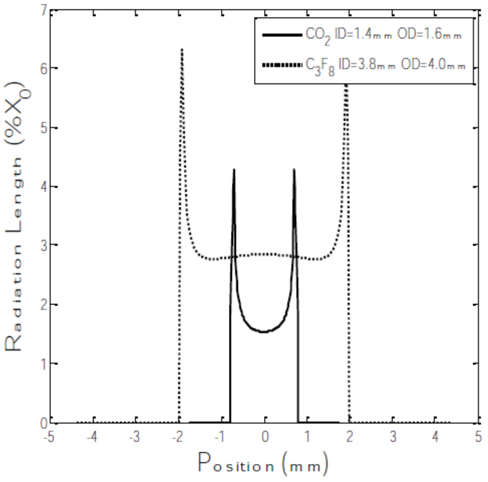
100 bar pressure tested Tubes, 50μ wall thickness

Weight Layer1 42g + 7g CO_2

Upgrade: CO_2 cooling



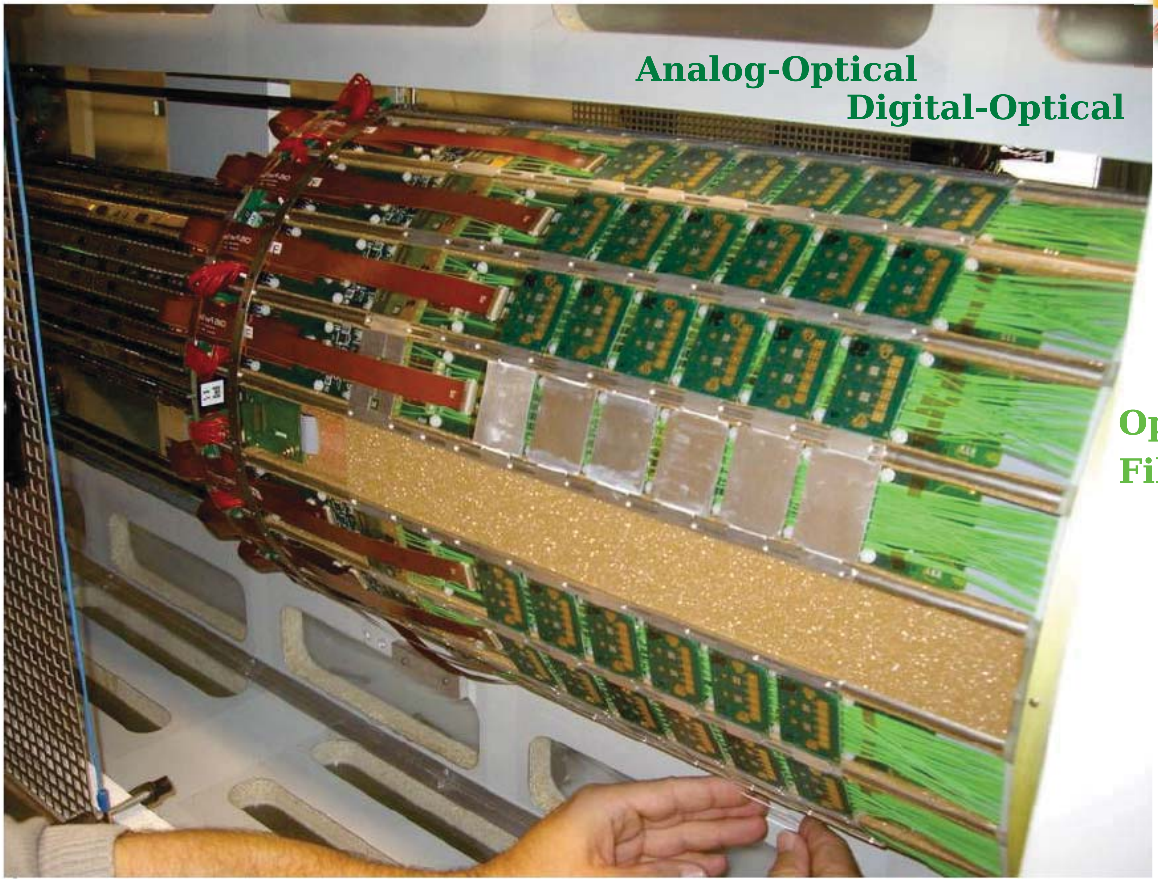




- 2-phase CO_2 cooling: large latent heat
- operating at -35°C, good viscosity
- reduces Si leakage current
- reduces defect activation in Si

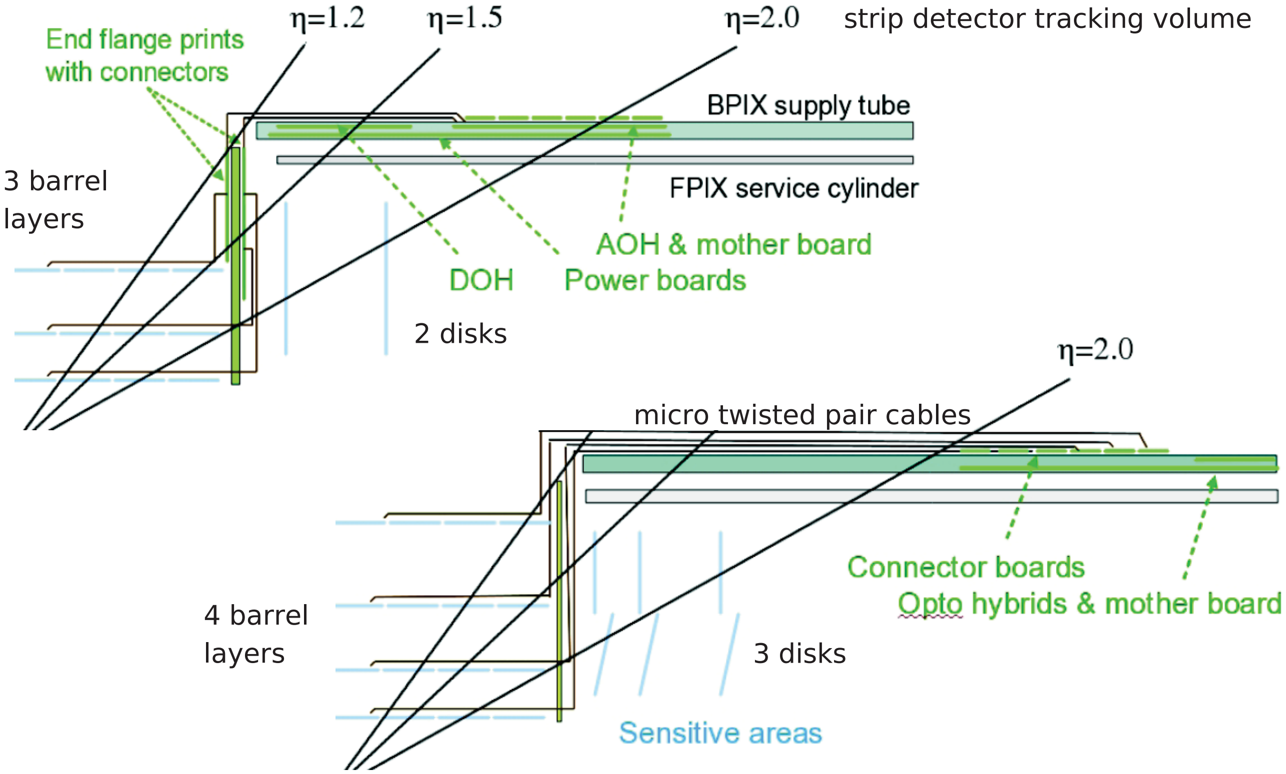
- Thin tubes, 50 bar
- material reduction

Barrel Pixel services

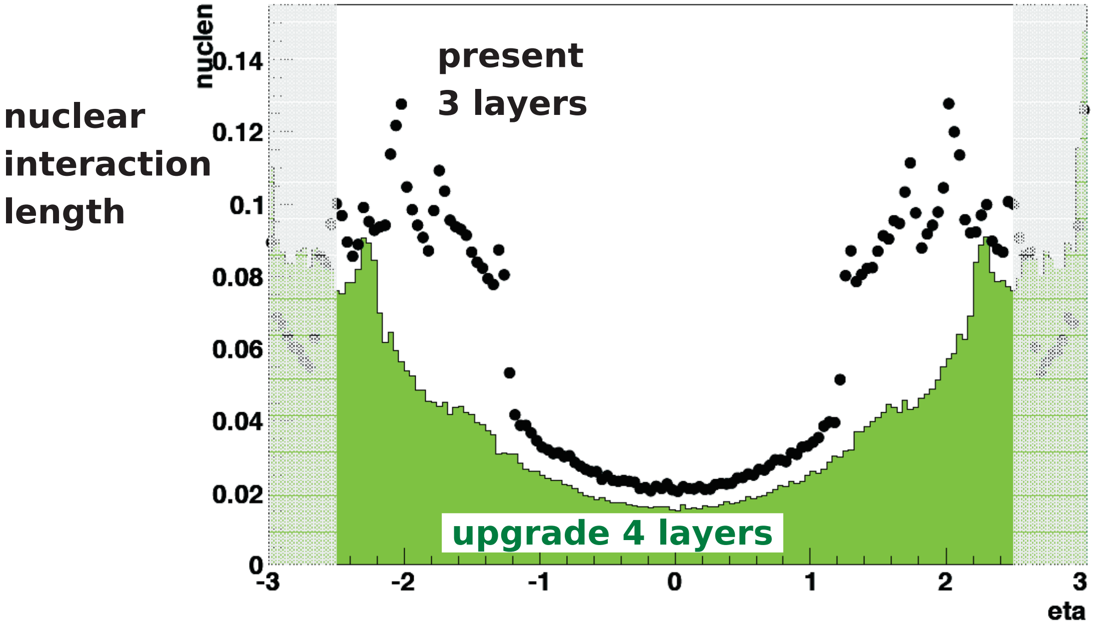


Optical Fibers

Moving readout material out of the tracking region



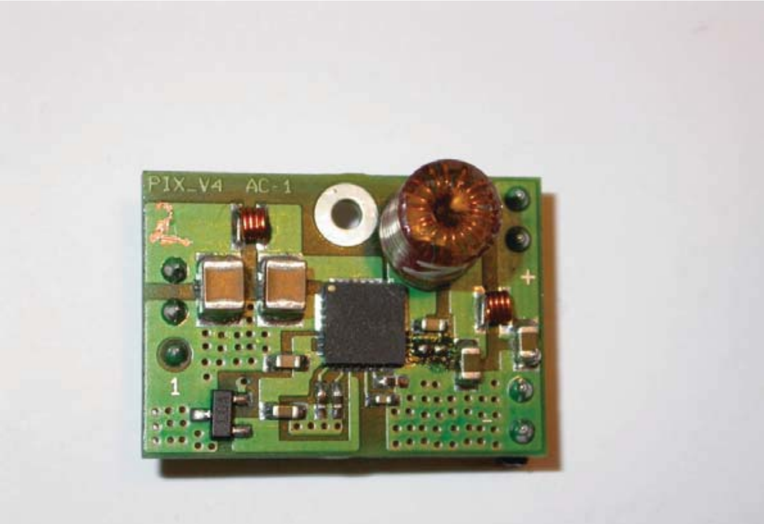
Barrel pixel material budget



Up to 12% of all hadrons are lost due to nuclear interactions in the present pixel barrel.

Upgrade will give up to factor 2 reduction.

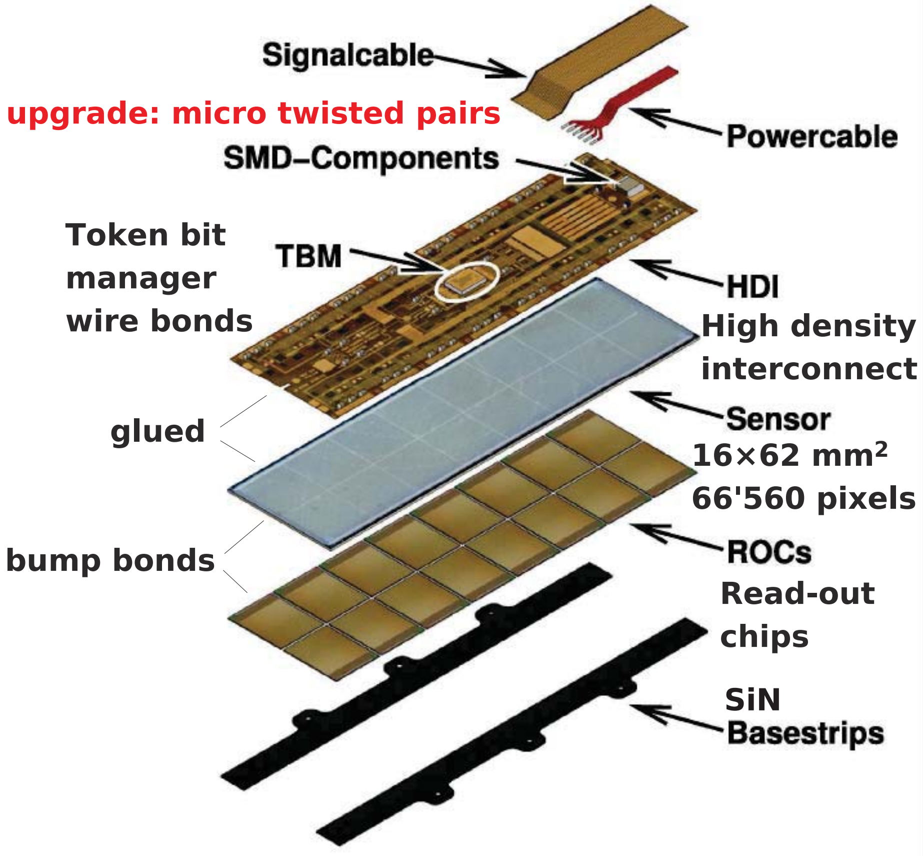
Services

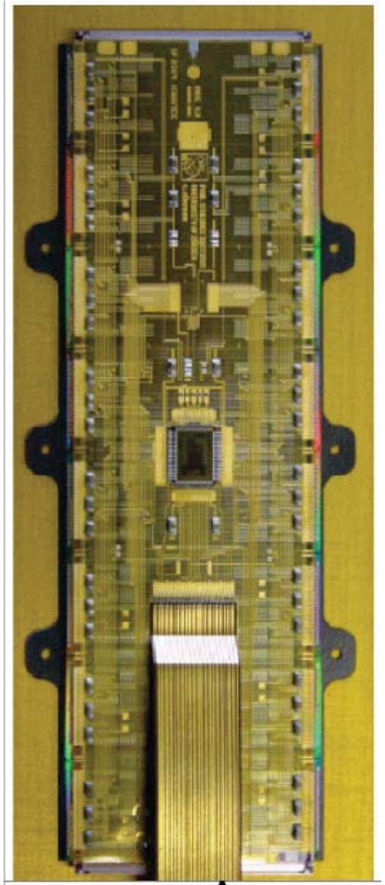


- DC-DC converter developed in Aachen:
  - air-core coil, 10V → 3.3 V, 3 A, η=75%
  - radiation resistant AMIS 2 chip (CERN), switching at 1.2 MHz,
  - optimized design for low noise.

- CMS tracker cable channels are full:
  - have to use the existing services.
- Optical fibers:
  - go from 40 MHz analog to 320 MHz digital readout.
- Power:
  - Use DC-DC converters at the detector.
- Sensor bias:
  - 600 V → 1000 V.
- CO2 cooling:
  - pipe-in-pipe for 100 bar.

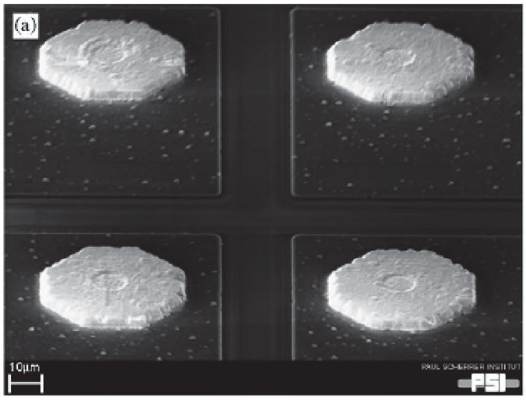
CMS barrel pixel module



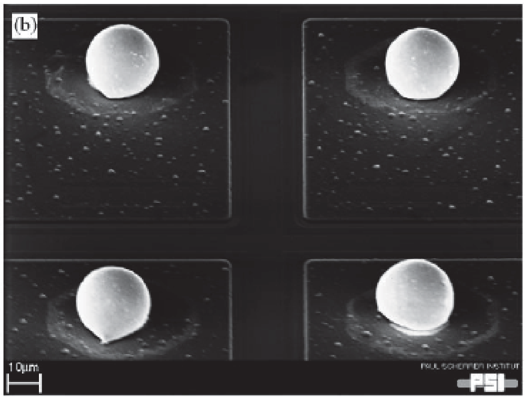


full–module ≙ 16 ROCs

Bump bonding at PSI



Indium pads deposited on the Si sensor.

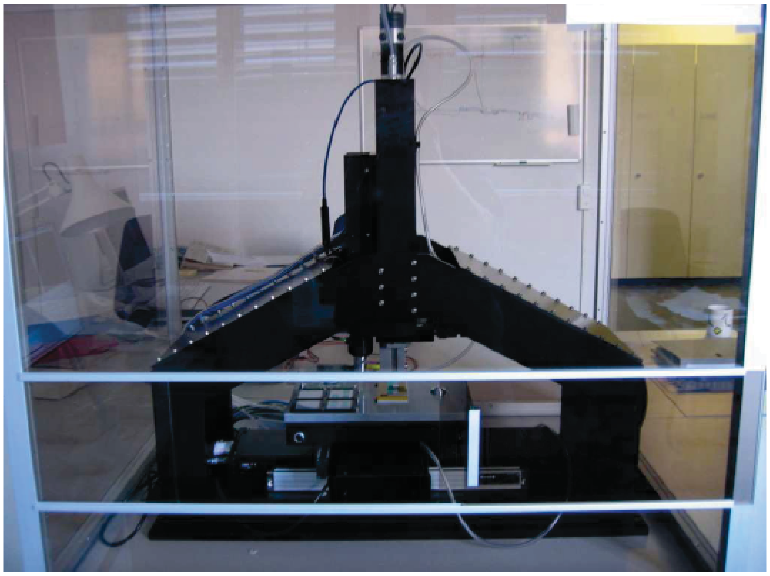


After re-flow at 150°C in N_2 and CH_2O_2 atmosphere.
15 µm diameter.

Involves many steps:
sputtering,
photo lithography,
etching…

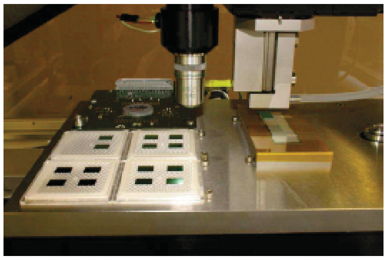
Ch. Broennimann et al.: Development of an Indium bump bond process for silicon pixel detectors at PSI
NIM A565(2006)303-8

Flip chip assembly at PSI

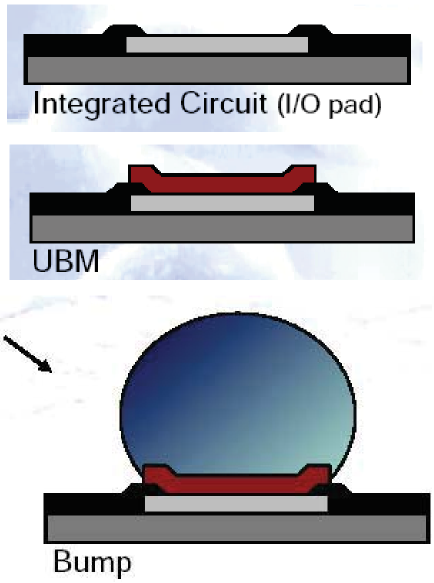


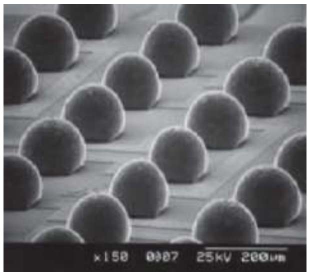
Precision *x*-*y*-*z* stage
Computer controlled
Commercially available.

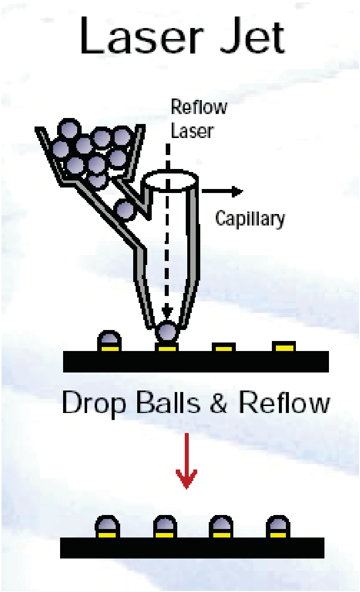
- Precision: $1 \div 2\,\mu\mathrm{m}$
- Production rate:
  - 6 modules / day + tests
  - automated: 1 hr/module
- Bare module test:
  - IV-curve
  - ROC functionality
  - bump yield
  - rework: 80% success



Alternative



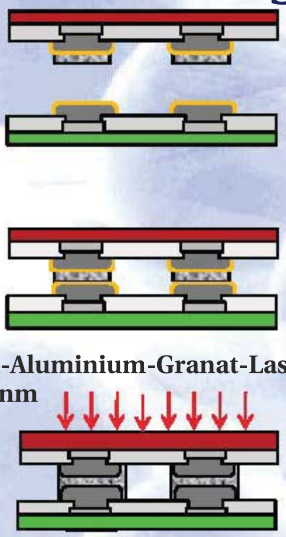




- Start with high-precision balls.
- Drop through capillary towards pad.
- Melt by laser pulse during fall.
- Solidify on pad.
- Step-motor controlled.
- 5 ball / second.
- 40 µm balls at 80 µm pitch possible now.
- 30 µm balls under development.

http://www.pactech.de/index.php?option=com_content&view=article&id=154&Itemid=21 68

Laser reflow bonding



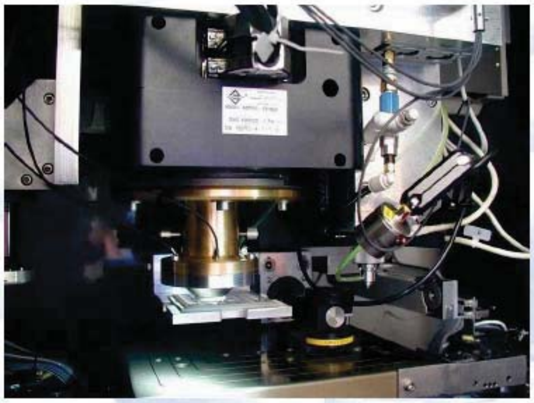
1) Pickup Die & Align
(±5 µm)

2) Contact
(10kgf)

Neodym-dotierter Yttrium-Aluminium-Granat-Laser
1064 nm

3) Laser Reflow
(20msec, Nd+3YAG)

LaPlace Assembly System™ PacTech

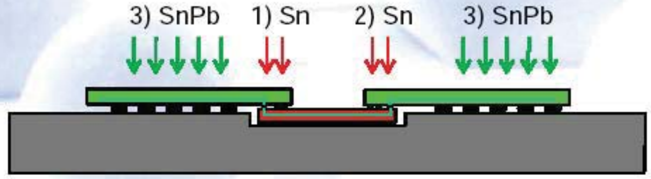


Placement accuracy: +/- 15um: 3000 - 5000 UPH
Placement accuracy: +/- 10um: ~2000 UPH
Placement accuracy: +/- 5um: ~1000 UPH
Placement accuracy: +/- 2.5um: ~500 UPH

units per hour

Laser based assembly allows localized heating:

- Selective to individual die
- Energy localized to bumped areas
- Ability to differentiate between solder alloys
- Low stress
- Minimizes IMC (time/temp)



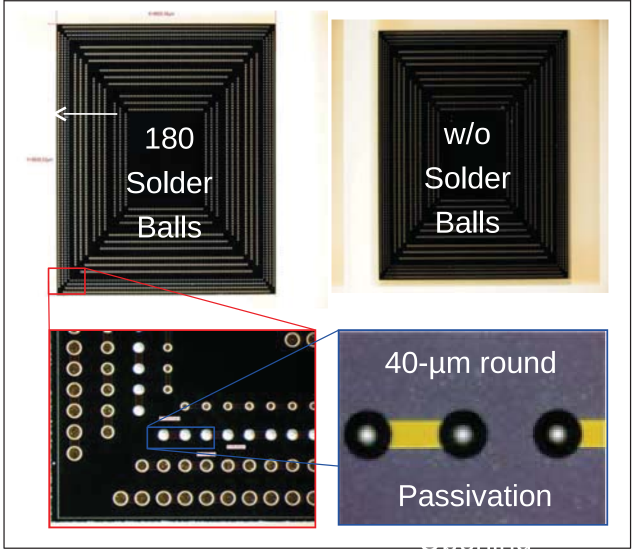
Mp SnPb = 183°C Mp Sn = 232°C

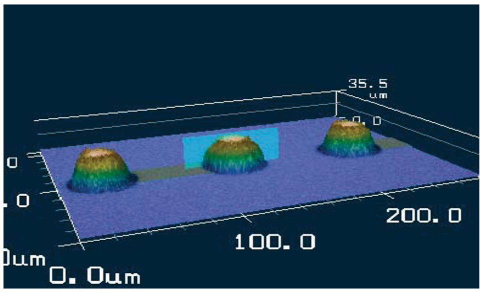
PacTech publication 66 Nov 2009

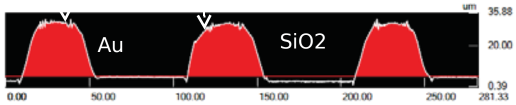
PacTech test structures

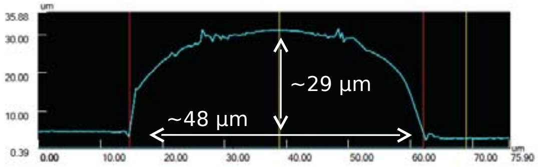
Pac 2.7 Wafer from Pac Tech GmbH

- Two 200-mm Wafers with 275 Chips each
- 5-µm electroless Ni/Au UBM on both
- 40-µm SAC305 Solder Jetting with SB2 on one
- Wafer Sawing & Chip Singulation









Available since Dec 2010.
Used with 4 machines/vendors.

Karsten Hansen, DESY FEC

Pac Tech: SB2 Jet

Solder Ball Placer:
pre-formed balls are placed sequentially at 6-7 Hz
fused by laser heating
30 µm balls being certified, 40 µm ordered for test.

SET: FC 150 **Flip-chip bonder**

Industry standard, expensive, slow.
For placing and re-flow heating. Used at IZM.

SET: Kadett K1

Unitemp: RS-350-110

PSI design: cheapest, slow.
no > 50 mm heating chuck available.
Tacking Tests completed on small samples:
> 0.6 g/ball @ 155°C for chip & substrate.
Re-flow tests completed: OK.

Pac Tech: Laplace

RFA 300M

Reflow Oven RFA 300M

Novel Industry Standard: medium price
laser-assisted, fast.
Tacking Tests completed:
low force with chip at 195°C for 1s.
Reflow Tests completed: OK.

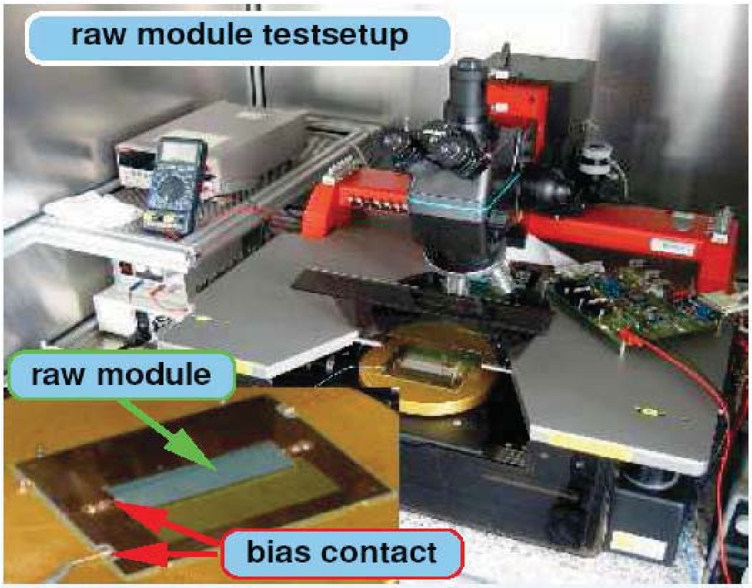
Finetech: FINEPLACER femto

Novel FC 150 competitor: medium price.
Placing and re-flow heating, low-force, fast.

Tacking / re-flow tests under way.

Karsten Hansen, DESY FEC

Bare module test at PSI



Semi-automatic probe station at PSI:
load manually,
step and measure automatically.

- Test bare module after flip-chip bump bonding:
- Sensor I-V curve.
- Test 16 readout chips.
- Determine bump yield.
- Rework bad modules:
  - replace individual chips.

Probe station at DESY FEC

Süss Microtech PA 300 Probe Station

auctioned
from
Qimonda
in Dec 2009

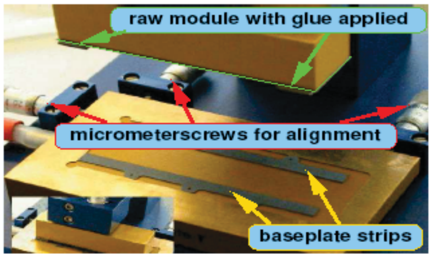
Probe-Card Holder

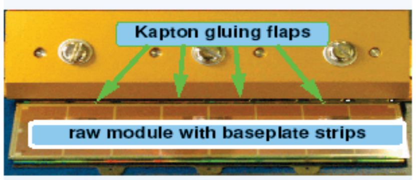
will order 42 needle probe card for testing ROCs after bump bonding.

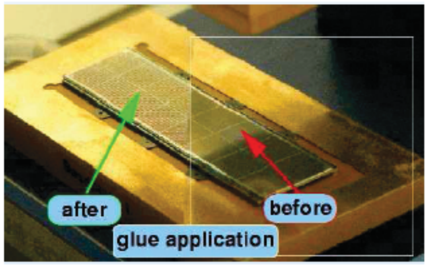
up to 300 mm wafers
Semi-Automatic
Shielded
Thermo chuck -40 .. +125°C

Barrel pixel module assembly line at PSI

- Production rate:
  - 4 full + 2 half modules / day
  - or 6 full modules / day
- Three glueing steps:
  - glue basestrips to raw module
  - underfill sensor with glue
  - glue HDI to complete assembly
- Important: custom-made tools

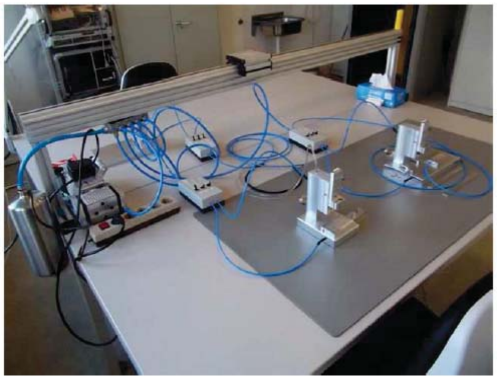




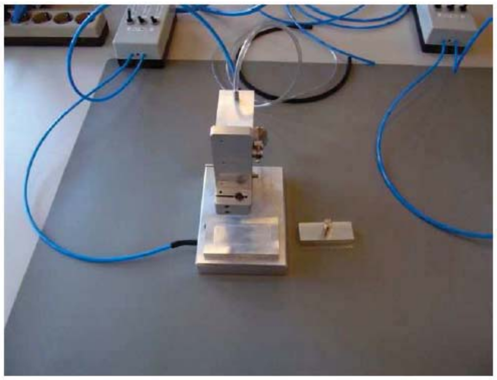


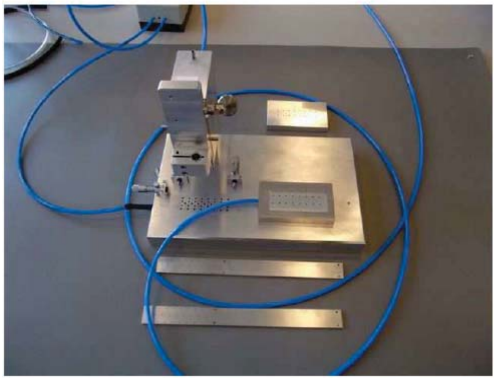
Tools and assembly line being prepared at Uni Hamburg.

Pixel module assembly tools at Uni HH



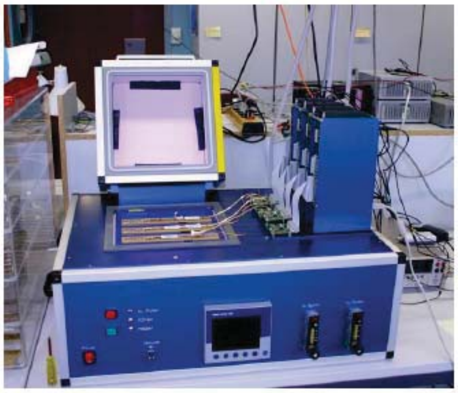
Tool rebuilt according to PSI CAD drawings. Gluing tests on dummy modules underway.

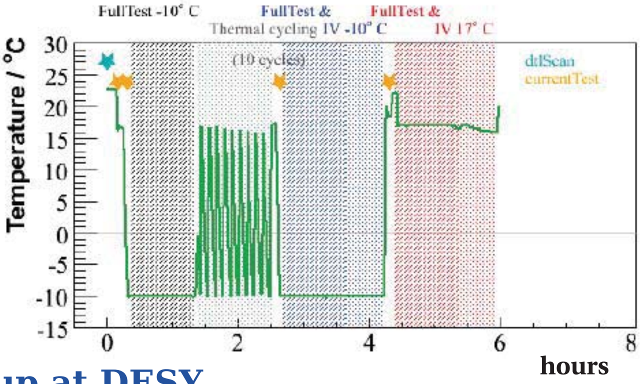




Pixel module cold calibration

- Challenges
  - Huge number of channels: 5 ÷ 6x10^7
  - Multy-dimensional parameter space: 29 DACs/ROC
  - Temperature dependence: tests done at -10°C and +17°C **upgrade: -20^{0}C**
- Test set up
  - Programmable cooling box
  - 4 modules at a time
  - Castom built test-boards with FPGA
- Procedure
  - Start-up adjustments
  - Full Test at -10°C
  - 10 thermal cycles
  - Full Tests and IV at -10°C and +17°C





Cold calibration set up will be set up at DESY.

Pixel gain calibration

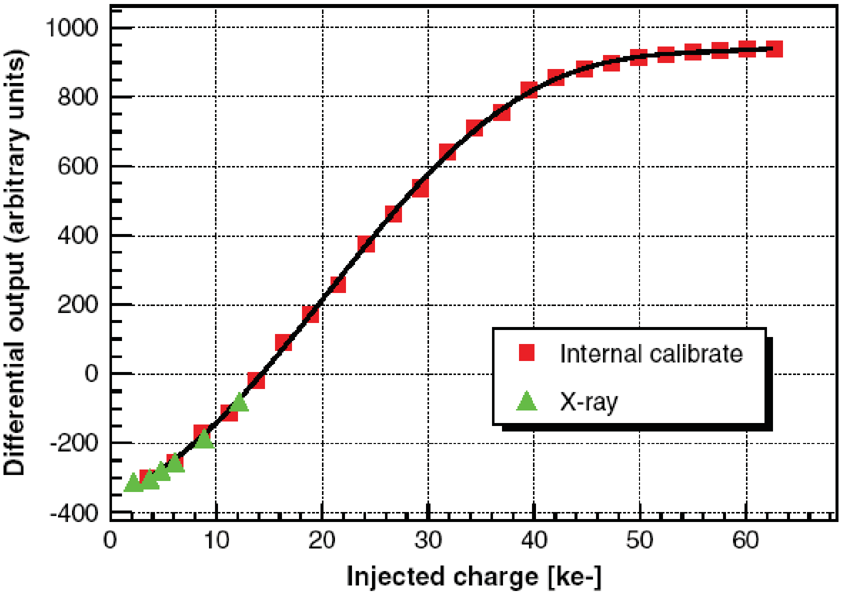


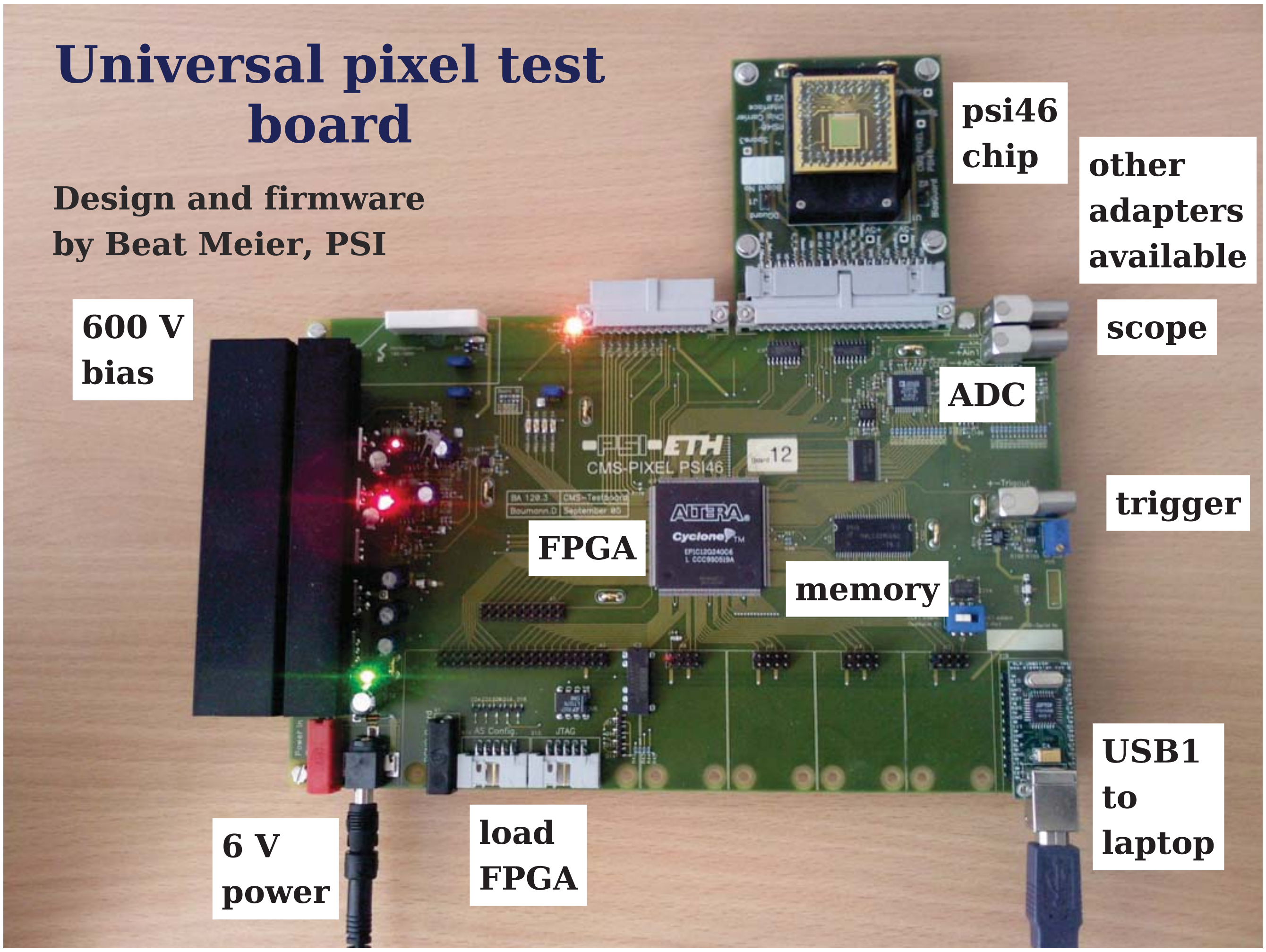
Fig. 8. Analog signal transmission.

H.C. Kästli et al., NIM A565 (2006) 188–194

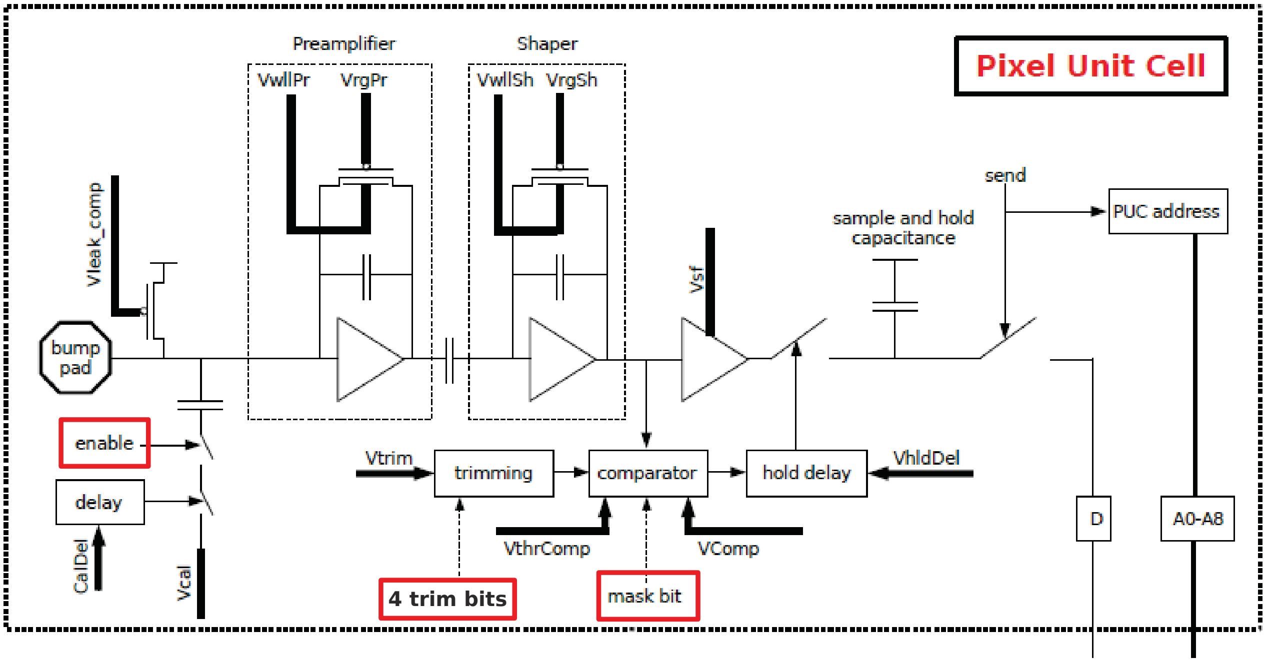
- Ultimate position resolution comes from pulse height interpolation.
- Need pixel-to-pixel gain calibration.
- Large amplitudes:
  - internal test pulse.
- Close to threshold:
  - X-ray lines (Mo, Ag, Ba).
- X-ray stand being prepared at Uni HH.

Universal pixel test board

Design and firmware
by Beat Meier, PSI



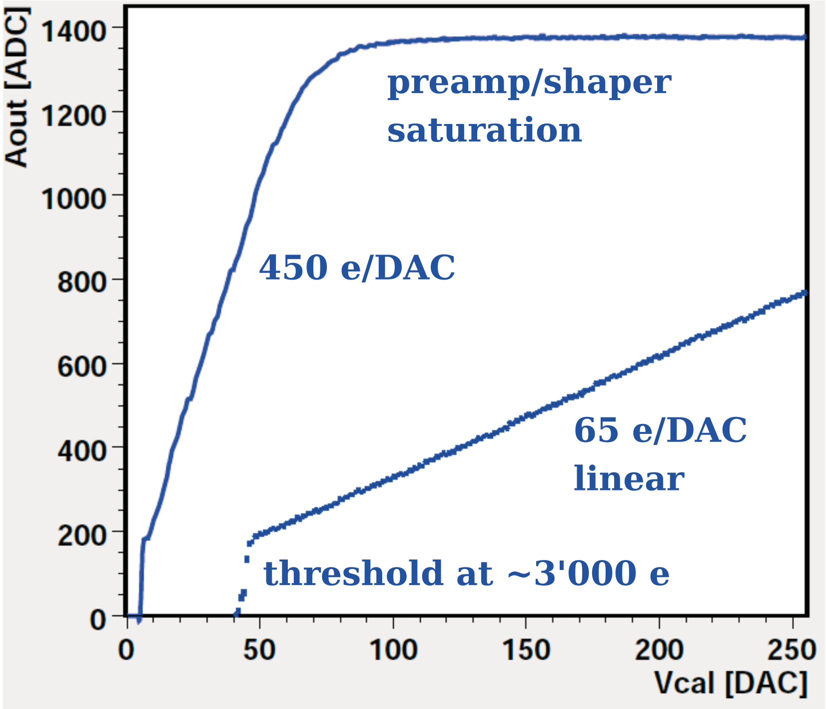
psi46 pixel readout chip



━ adjustable by programmable DAC, 26 per ROC

☐ programmable register, 3 per pixel

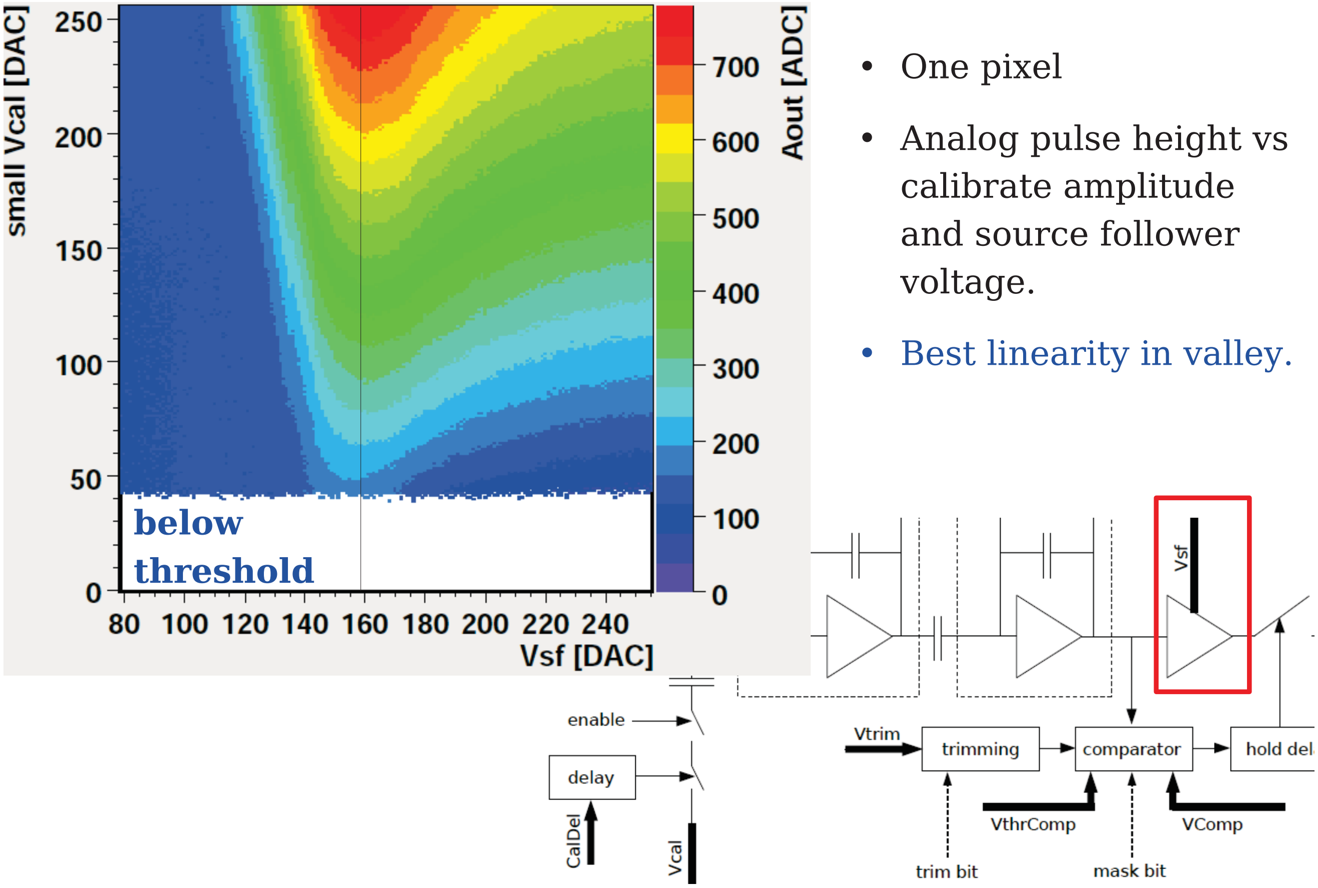
gain and linear range



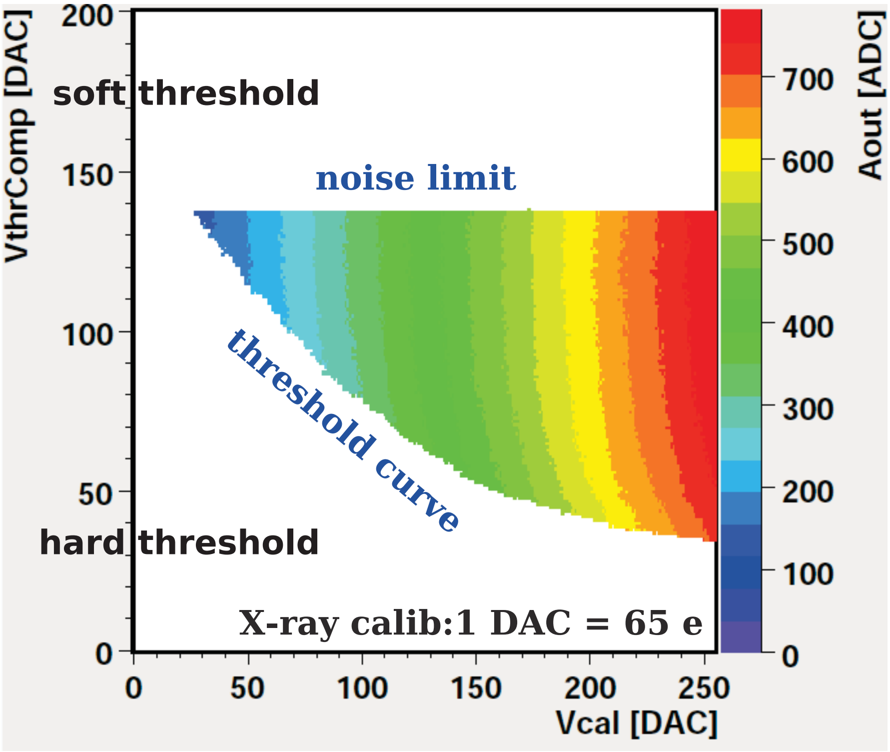
- One pixel.
- 2 Vcal ranges (PSI X-ray calibration):
  - CtrlReg 0 or 4,
  - 65±5 e/DAC,
  - 450 e/DAC.
- Linearity for small pulses important for spatial resolution using charge sharing.
- Saturation around 36'000 e (~1.6 MIP).

Linear range vs Vsf

- One pixel
- Analog pulse height vs calibrate amplitude and source follower voltage.
- Best linearity in valley.



Comparator threshold

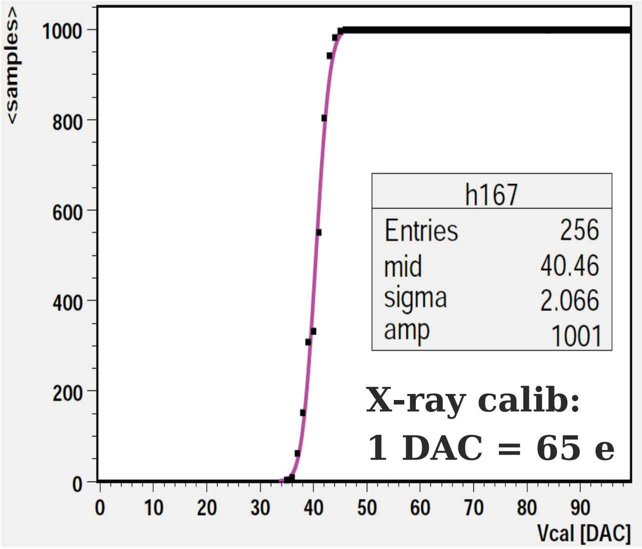


- One pixel
- Analog pulse height vs threshold and calibrate amplitude.
- White region:
  - no signal.
- Colored bands are not vertical:
  - time walk.

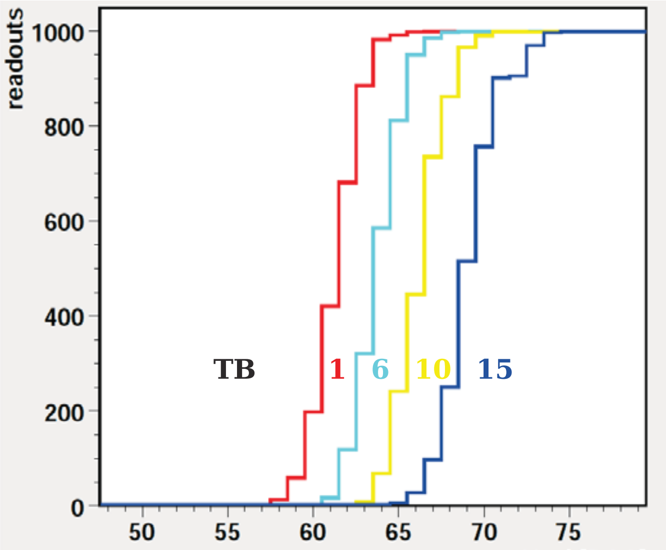
Threshold curve

one pixel

vary test pulse amplitude



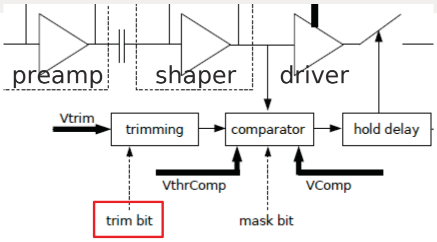
vary trim bits



threshold broadened by noise

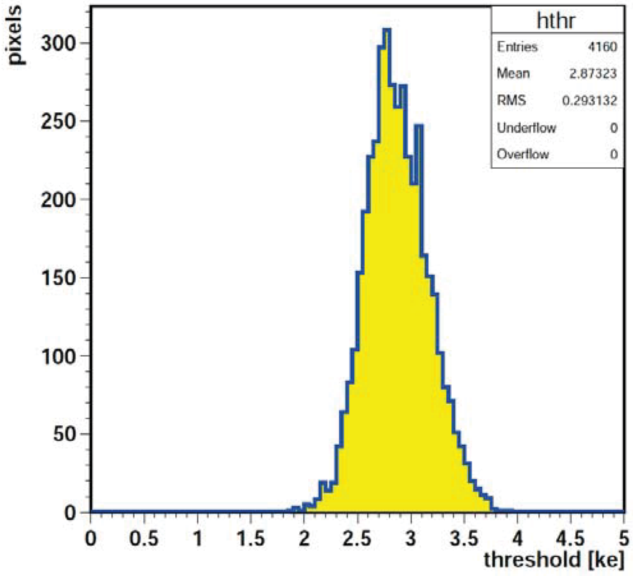
fit by error function

noise: 130 e



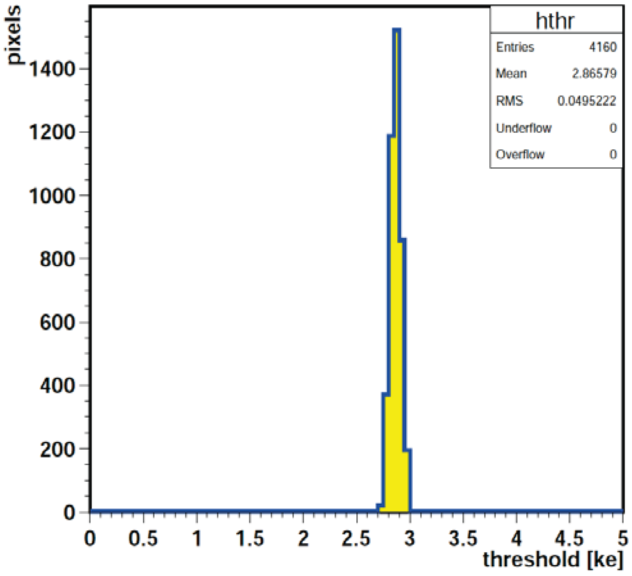
Threshold variation

4160 pixels / cip



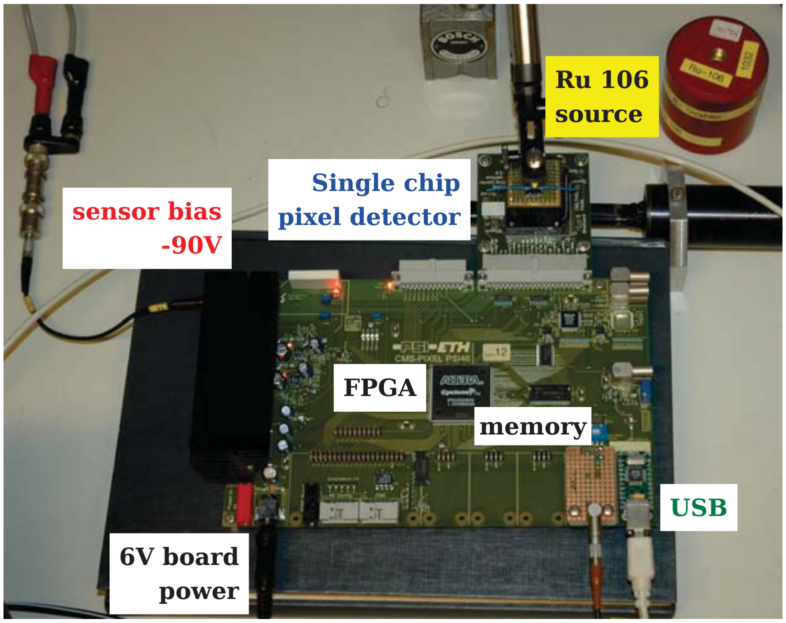
CMS transistor variations:
threshold spread 290 e

the same chip, trimmed:



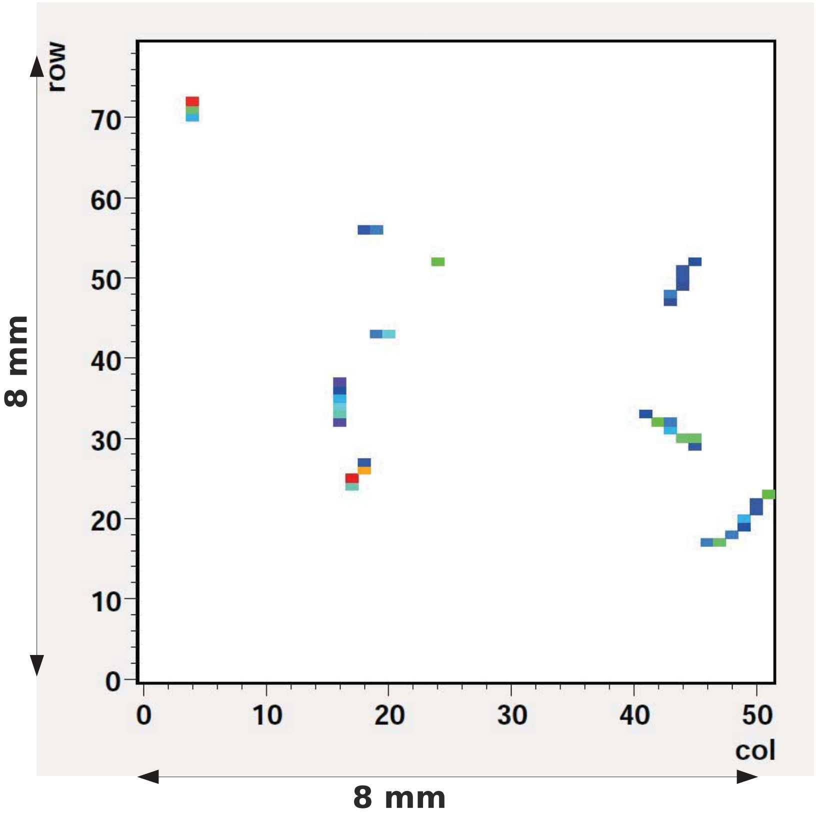
4-bit DAC trimming:
threshold spread 50 e

Source test setup



- ^{106}Ru source mounted above the chip:
  - Activity ∼14 kHz,
  - electrons up to 3.5 MeV.
- FPGA:
  - data clock cycle stretched up to 1 ms,
  - trigger,
  - readout,
  - store in memory.
- Final readout by USB.

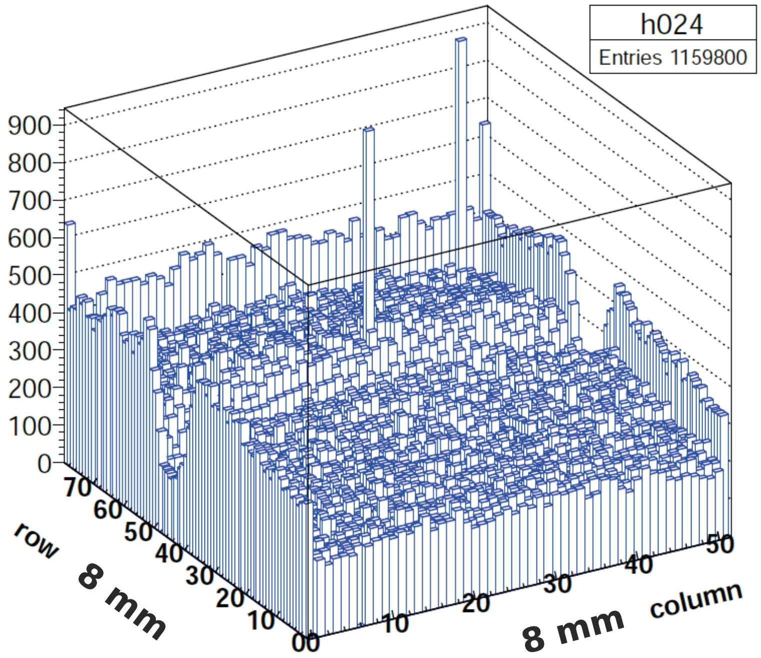
Source test event display



- A single event integrating over 1 ms:
  - ~15 hits per trigger
- Low energy electrons:
  - Scattering in the source holder,
  - wide angles of incidence,
  - large clusters.
  - tracks visible.
- Clusters of pixels identified by software.

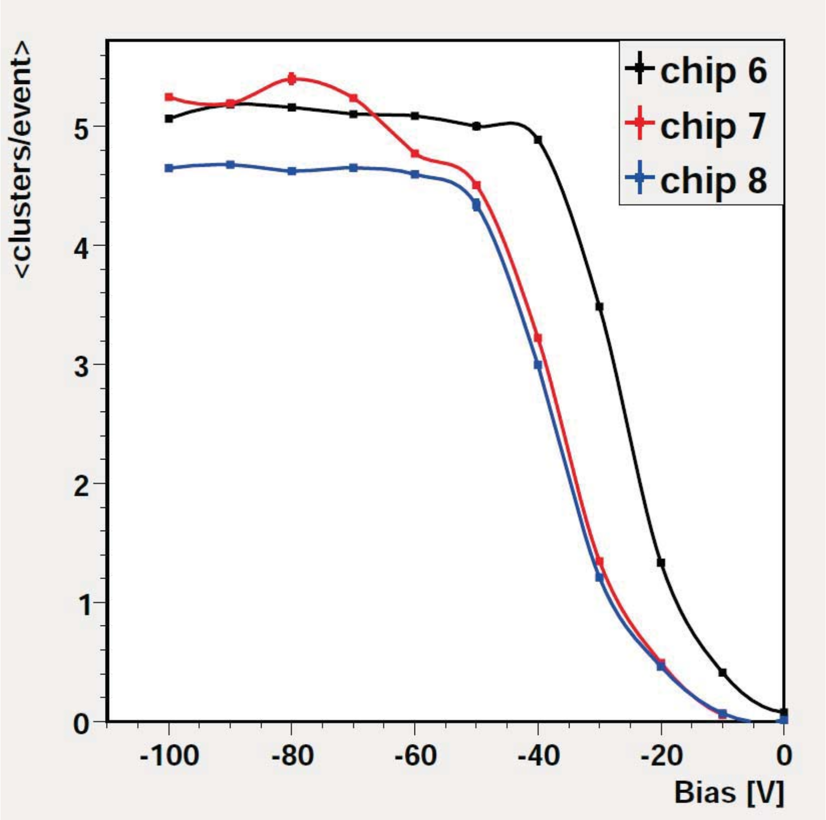
---

hit map



- Ru source, 100s.
- Wire placed across the chip.
- Pixel map (φ-z):
  - shadow of the wire
  - 2 noisy pixels.
  - long and/or wide pixels at 3 edges.

Cluster multiplicity vs. bias voltage

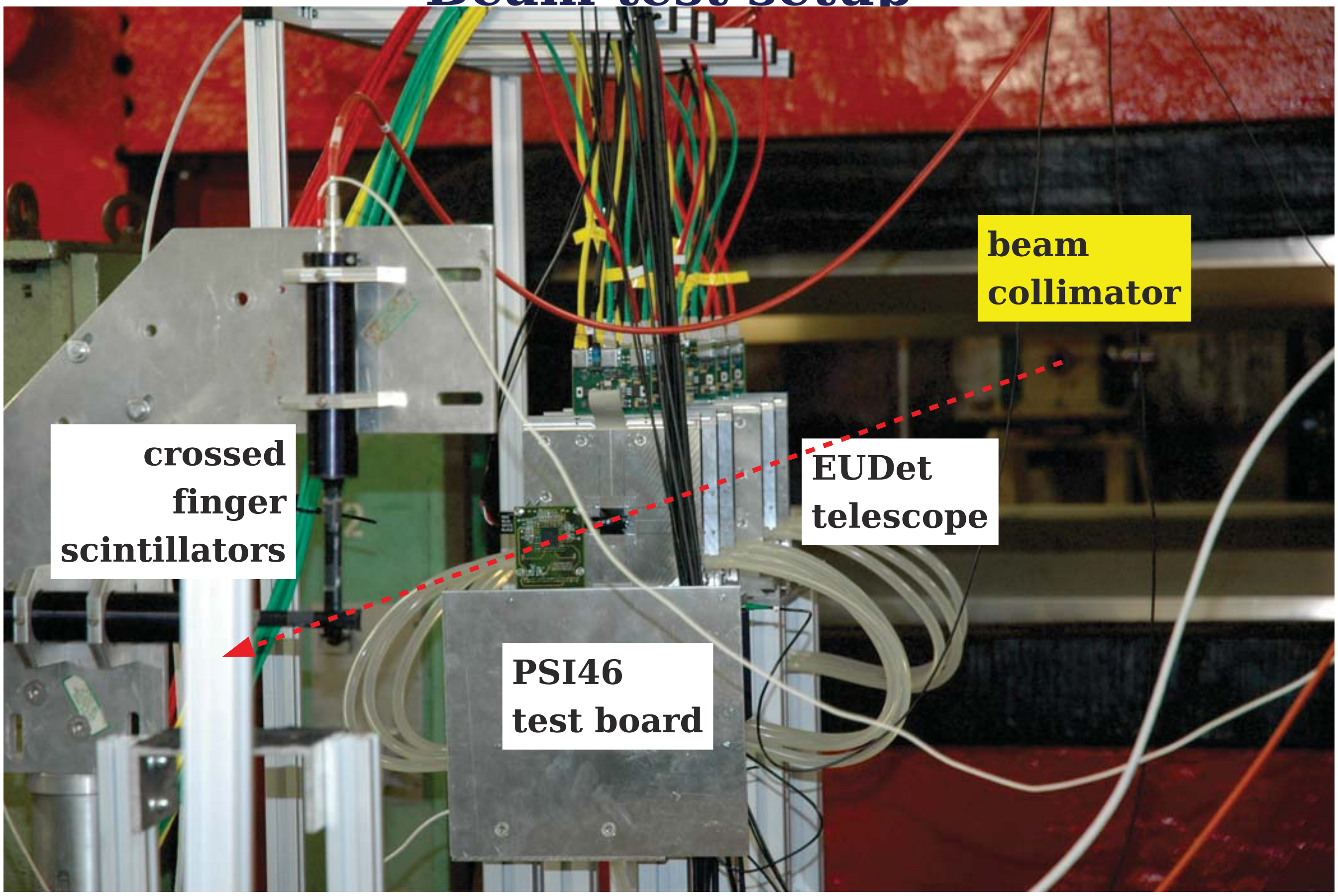


- Ru106 source.
- All scans with:
  - Internal trigger
  - Clock stretch 1 ms
  - 10s run for one Vbias value
- Cluster efficiency saturates below -50 V.
- Plateau variation:
  - Source position,
  - Thresholds.

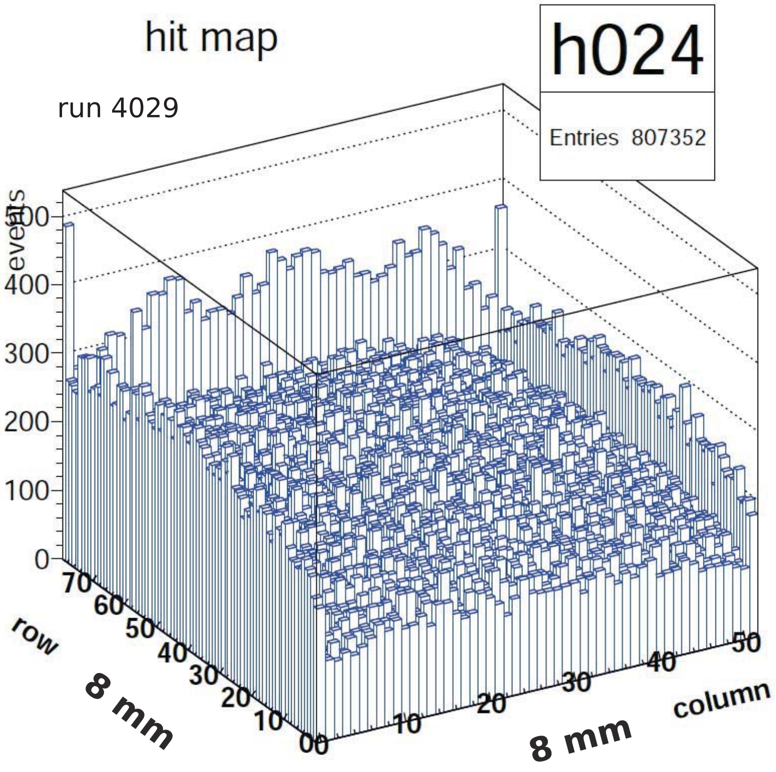
DESY II


http://adweb.desy.de/~testbeam

Beam test setup

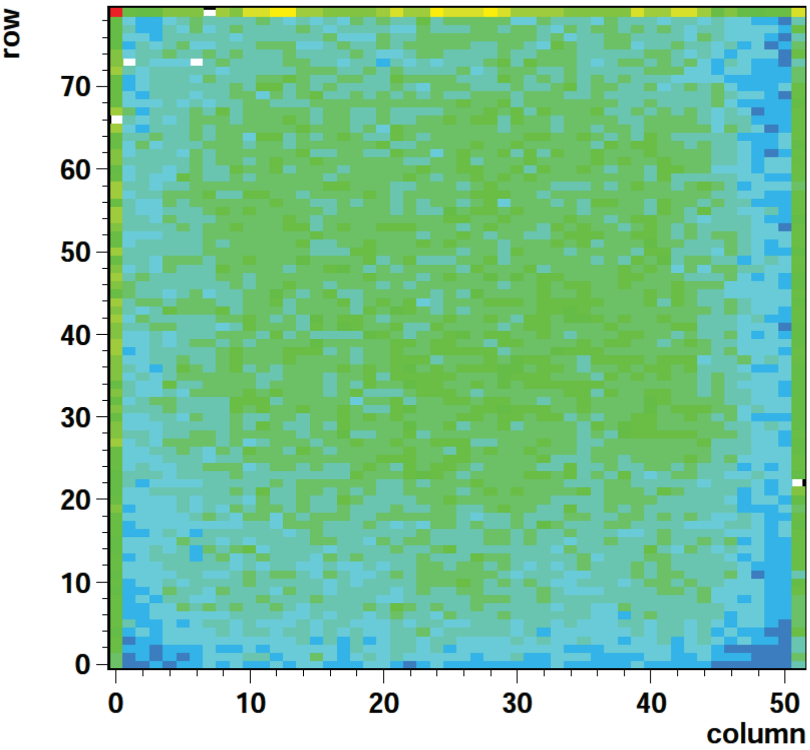


Pixel hit map



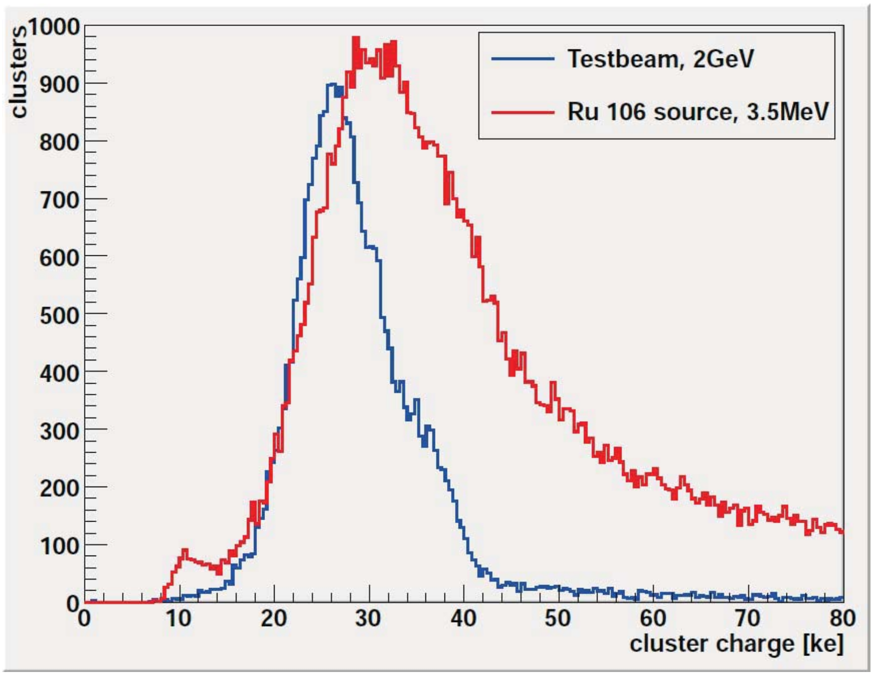
- 2 GeV e^+ beam.
- After space and time alignment:
  - 4 kHz coincidence rate
  - Fill test board memory: 60MB in 3.5 min.
  - USB transfer takes another ~2 min.
- One chip fully illuminated.
- Border pixels have double size and rate
- Corner pixels have quadruple size and rate

Pixel hit map



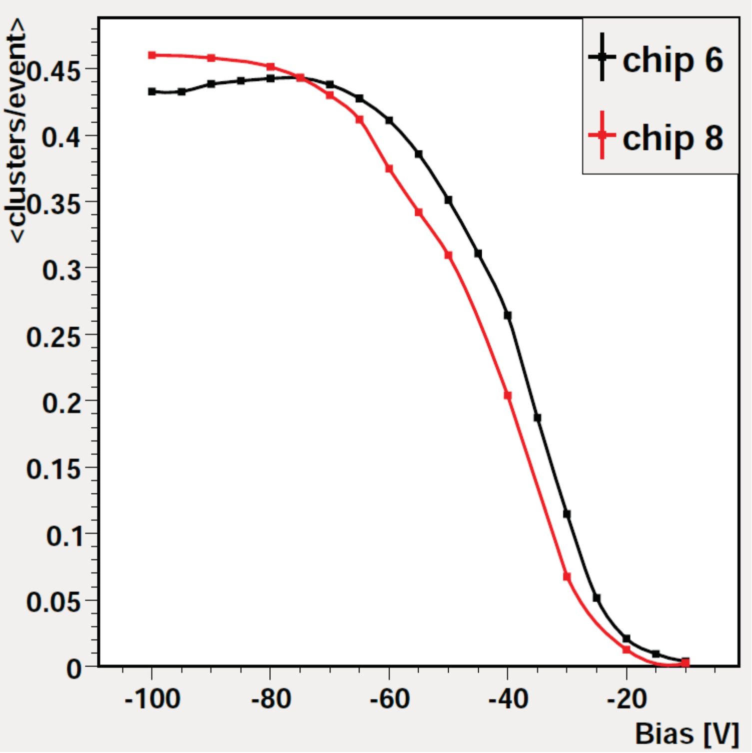
- the same run
- a few dead pixels
- non-uniformity:
  - beam profile,
  - misalignment between sensor and scintillator,
  - limited trigger region (~1 cm^2) just enough to cover 0.8×0.8 cm^2 chip.

Cluster charge: Ru source vs beam



- Chip 8, -90V bias, Vthr 100
- 2 GeV e+ test beam:
  - Minimum ionizing particles
- Ru 106 source:
  - long tail of stronger ionizing electrons (not fully relativistic).

Cluster multiplicity vs bias voltage



- 2 GeV e^+ beam.
- Cluster efficiency saturates below -80 V:
  - Need more bias voltage to reach full efficiency for minimum ionizing particles.

Project time line

- Produce assembly tools since 2010
- Develop assembly procedures 2011
- Develop testing and calibration procedures 2011
- Bump bonding tests 2010-2011
- Decide on bump bonding technique end 2011
- Contribute to ROC pre-series testing 2012
- Assembly and test procedures established 2012-201□
- Receive all components for series production 201□-201□
- Module assembly and calibration 201□-201□
- □th layer assembly and test end 201□
- Full system test at CERN 2016
- Ready for installation in CMS end 2016

Work Packages □□ □ □C□ □

□th layer: □□□ modules □ □□□ spares □ □□ rejects □ □□□

task	quantity	DESY	HH	Ka	Ac
sensors I-V	700		350	350	
bare module test	700	350		350	
bond TBM to HDI	700	350		350	
glue HDI to sensor	700		350	350	
bond ROCs to HDI	400k	200k		200k	
module testing	700	350		350	
cold calibration	700	350			350
X-ray calibration	700		350		350
layer assembly	1	1			
layer system test	1	1			
DC-DC converters	2200				all

People at □ □□□□ a□□ □ □□□ amburg □□□□□

- DESY:
  - Günter Eckerlin, deputy CMS group leader, DPix coordinator
  - Daniel Pitzl, pixel upgrade project leader
  - Carsten Niebuhr, Doris Eckstein, staff
  - Maria Aldaya, Jan Olzem, Alexey Petrukhin, Hanno Perrey, postdocs
  - Karsten Hansen, Jan Hampe, staff FEC
  - Carsten Muhl, Holger Maser, engineering
- Uni Hamburg:
  - Peter Schleper, professor
  - Georg Steinbrück, staff
  - Thomas Hermanns, postdoc
  - Lutz Berger, technical support

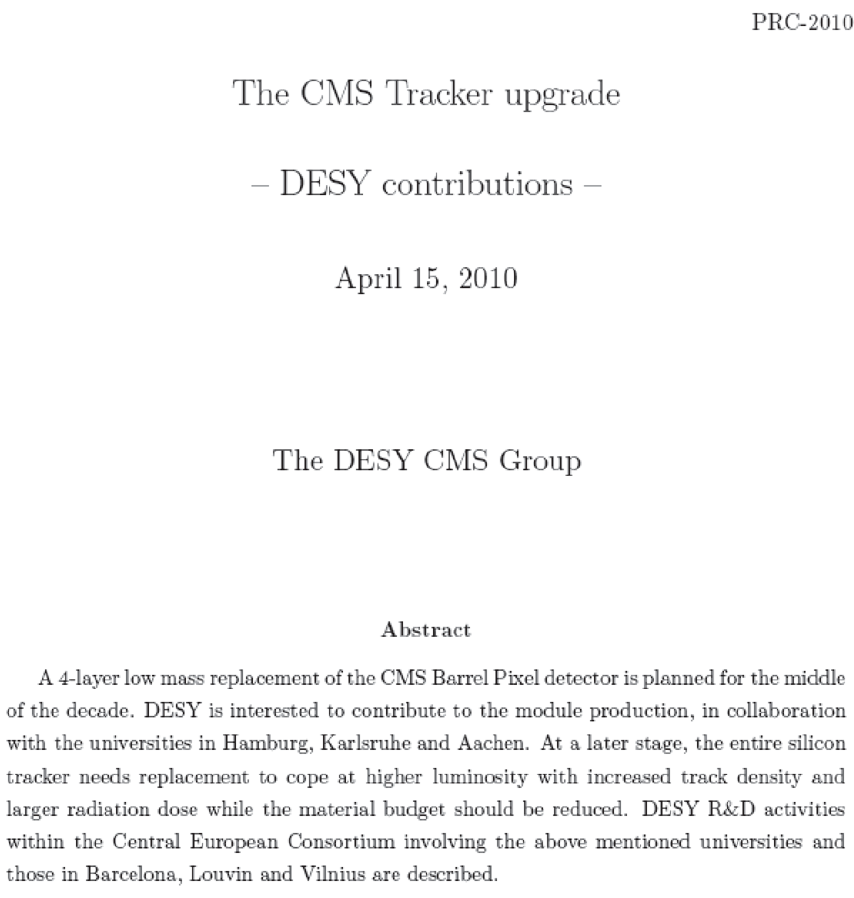
Summary

- The present CMS pixel detector is working very well and is an essential tool for track reconstruction and vertexing.
- The LHC luminosity is expected to exceed $10^{□□}$ /cm^{2}s in this decade:
  - the present pixel readout chip will become inefficient.
  - at least the inner pixel layer has to be exchanged after 2□0 fb^{-1}.
- □ □-layer replacement with a new readout chip has further benefits:
  - Better resolution, efficiency, and purity for pixel-based tracking,
  - Reduced material in the tracker volume with CO2 cooling, low mass design, services moved out of the tracking region.
- The German CMS institutes have been asked to contribute:
  - Design optimization and physics evaluation,
  - module assembly and testing,
  - DC-DC converter development and production.
- Preparations are underway.

Acknowledgments summer □□□□

- Aleksander □a□os
  - □□□□ summer student from Cracow
- □e□or □la□ov
  - □□□□ summer intern
- □eat □e□er □□□□□□□homas □e□ler □□□□□□ □□lma□ Rohe □□□□□:
  - for code and advice
- □lr□ch □oet□ □□□□□□:
  - for lab space, □□□ crate and modules, oscilloscope
- □la□□m□r □a□□ □□□□□□:
  - for the source
- Carste□ □uhl □□□□□□:
  - for the source holder
- □orste□ □□l□er □□□□□□:
  - for the □□□ trigger adapter
- □□gr□□ □regor □□□□□□test beam coordinator□:
  - for instructions and test beam hospitality
- □orbert □e□□ers □□□□□□test beam coordinator□:
  - for help with collimator and □□re target
- □amuel □ha□ar□a□ □□□□□□test beam support□:
  - for help with moving system and rate monitor
- □olger □aser □□□□□□:
  - for the test board support frame
- □r□□a □arutt□□□□□□□ a□□ □□□□□□□:
  - for the trigger scintillator and □□
- □□□□ □ach□□e □rou□:
  - for the steady test beam

Backup slides



PRC-2010-69-3

The CMS Tracker upgrade

– DESY contributions –

April 15, 2010

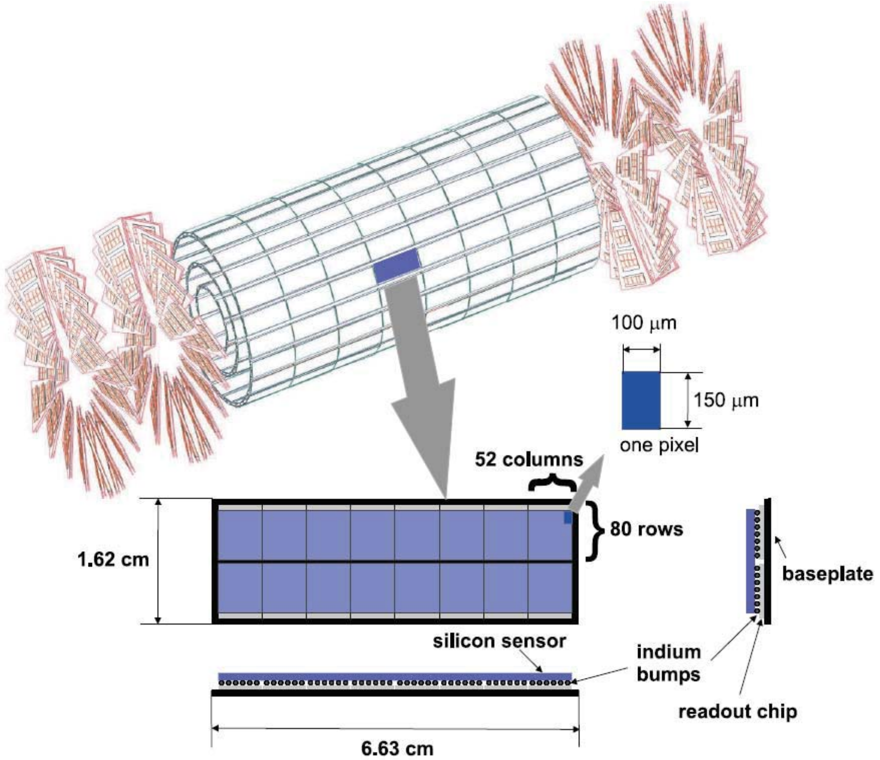
The DESY CMS Group

Abstract

A 4-layer low mass replacement of the CMS Barrel Pixel detector is planned for the middle of the decade. DESY is interested to contribute to the module production, in collaboration with the universities in Hamburg, Karlsruhe and Aachen. At a later stage, the entire silicon tracker needs replacement to cope at higher luminosity with increased track density and larger radiation dose while the material budget should be reduced. DESY R&D activities within the Central European Consortium involving the above mentioned universities and those in Barcelona, Louvin and Vilnius are described.

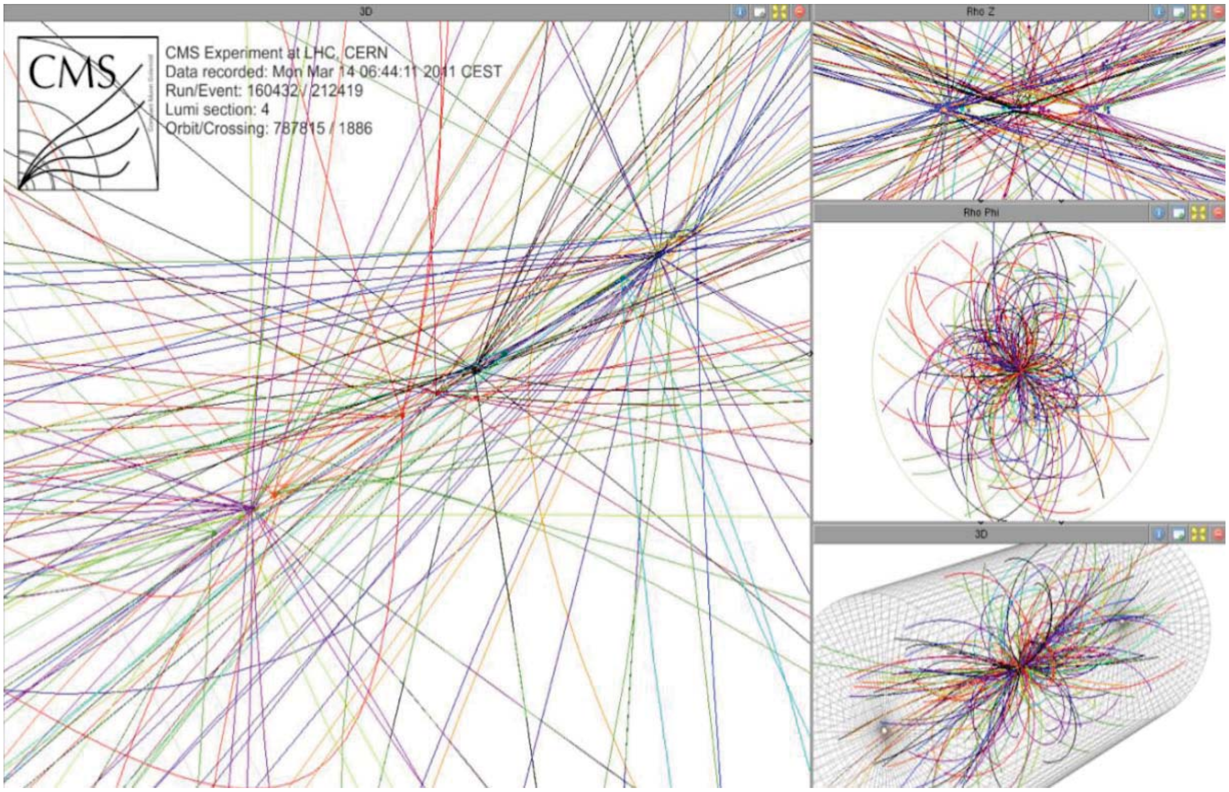
- DESY PRC document for the CMS Tracker upgrade.
- Pixel and Strips
- Hamburg and Zeuthen
- Submitted April 2010.
- Positive recommendation.

C□ □ □□□el



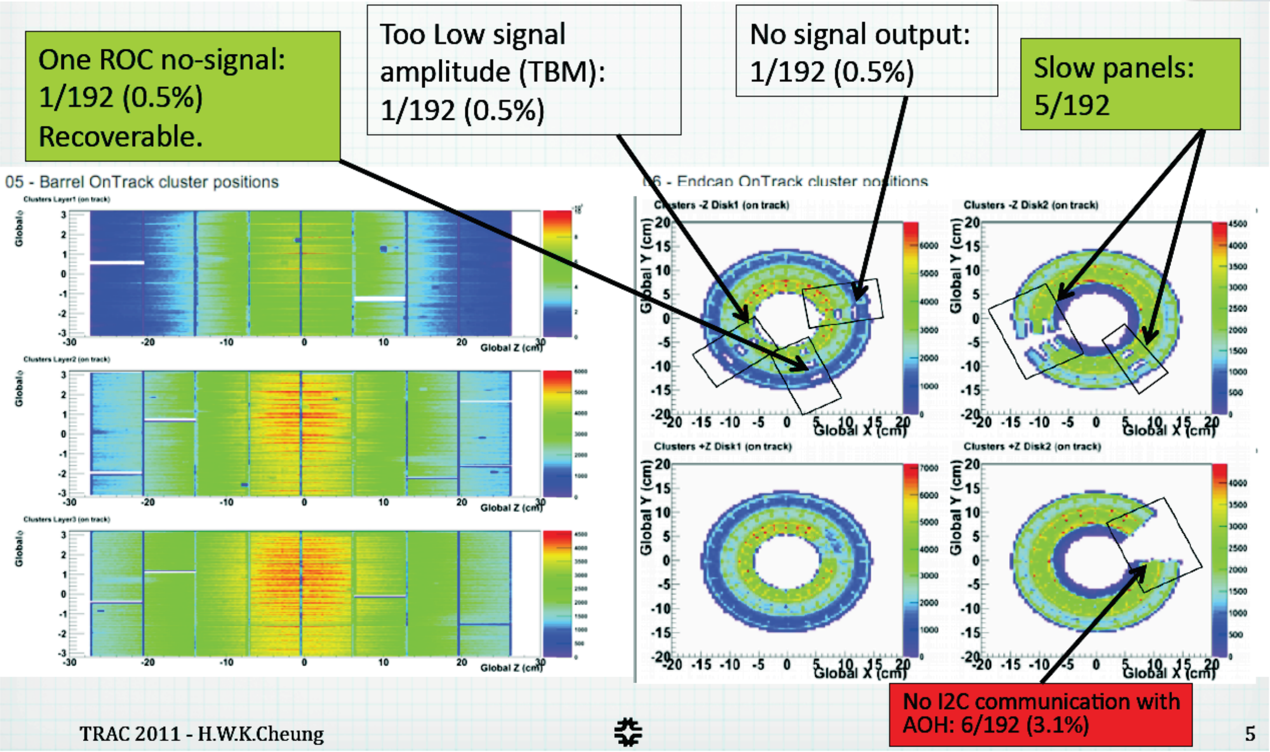
□. Doro□hov
Uni Zurich
200□

□□□□□ □ata



CMS Experiment at LHC, CERN
Data recorded: Mon Mar 14 06:44:11 2011 CEST
Run/Event: 160432 / 212419
Lumi section: 4
Orbit/Crossing: 787815 / 1886

Pixel operation in 2010



One ROC no-signal: 1/192 (0.5%) Recoverable.

Too Low signal amplitude (TBM): 1/192 (0.5%)

No signal output: 1/192 (0.5%)

Slow panels: 5/192

05 - Barrel OnTrack cluster positions

06 - Endcap OnTrack cluster positions

No I2C communication with AOH: 6/192 (3.1%)

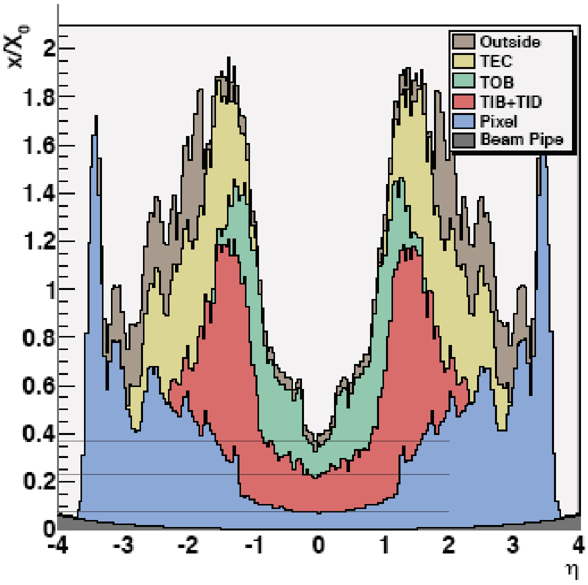
TRAC 2011 - H.W.K.Cheung

5

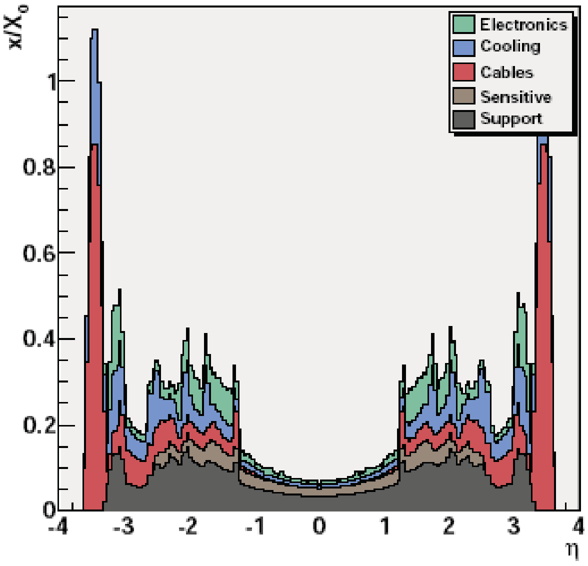
status end 2010

CMS tracker material

All trackers



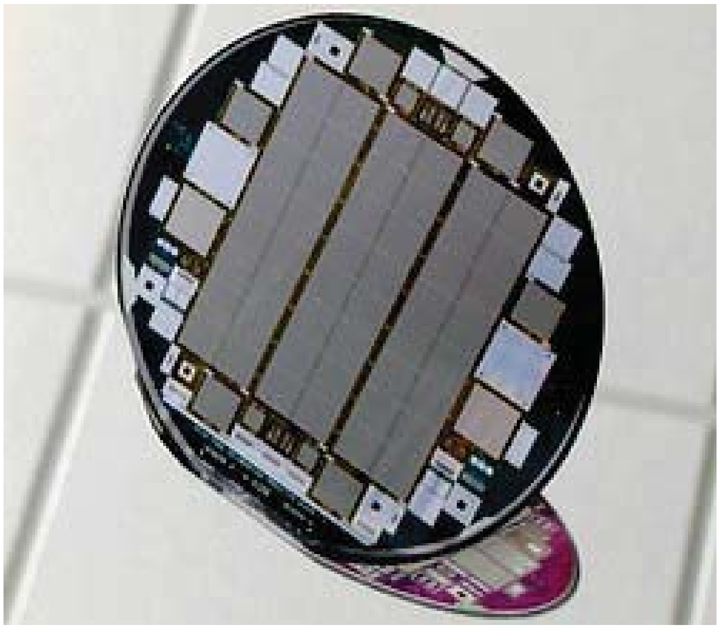
Barrel pixel



Upgrade:
factor 2 less in center
factor 4 less in endcaps

pixel note 2009

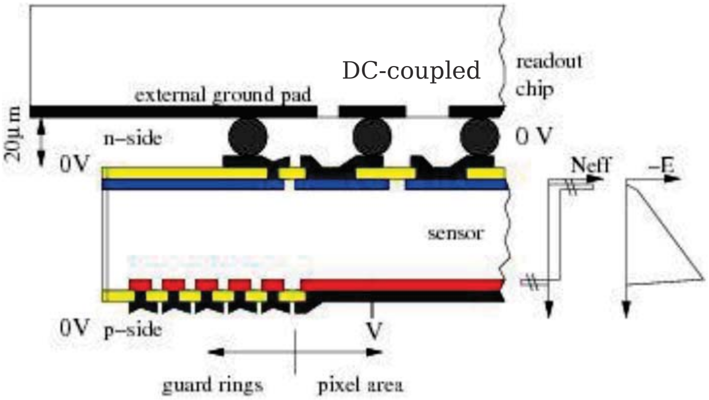
C[illegible] [illegible] Pixel Sensors



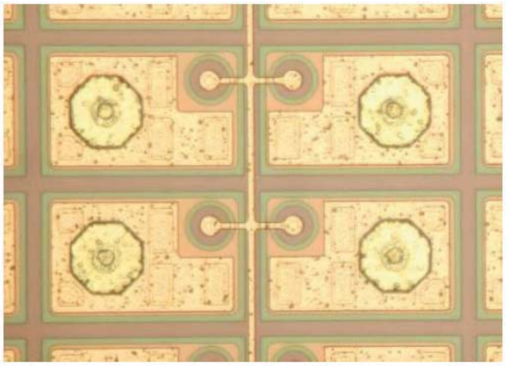
design: Tilman Rohe, PSI

- 60 wafers under production at CiS (Erfurt)
  - standard CMS pixel sensor design (double sided, n-in-n, p-spray insulation).
  - for Karlsruhe, [illegible] [illegible], CERN, Taiwan, MR[illegible], Purdue, DESY.
  - [illegible] wafers with increased bump pad passivation opening: [illegible]0 μm, for DESY.
  - Delivery in Feb 2012.
- Full sensors for first bump bondings.
- Single chip sensors for tests with new ROCs.

Pixel sensors

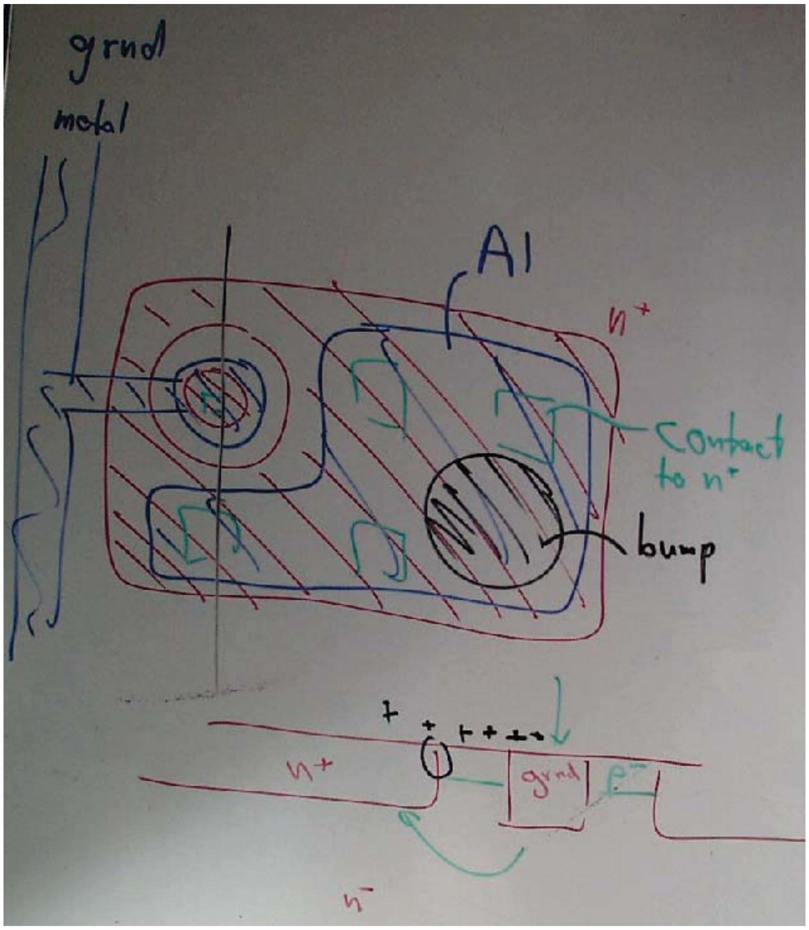


- Planar sensors, CiS Erfurt.
- 111-oxygenated float zone.
- n-in-n, p-spray insulation.
- collecting faster electrons:
  - larger Lorentz angle,
  - less trapping.
- pn-junction on back side (initially):
  - edges at ground,
  - double sided processing.



[illegible] [illegible]m [illegible]r[illegible] [illegible] [illegible] [illegible]m [illegible]

Grounding grid for testing before bump bonding



[illegible] pixel

[illegible] Rohe [illegible]
[illegible]
[illegible]c[illegible]g

CMS barrel and forward pixel sensors

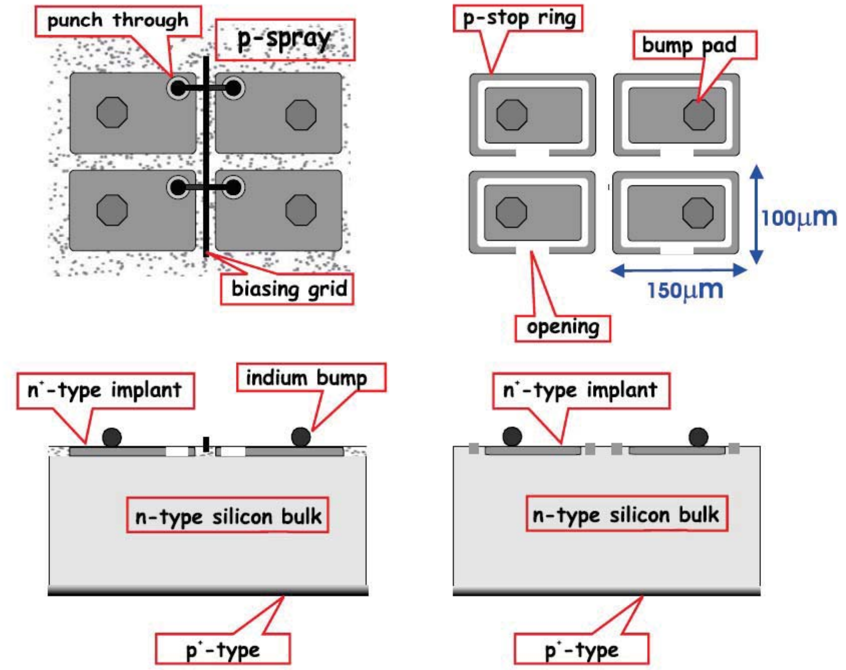
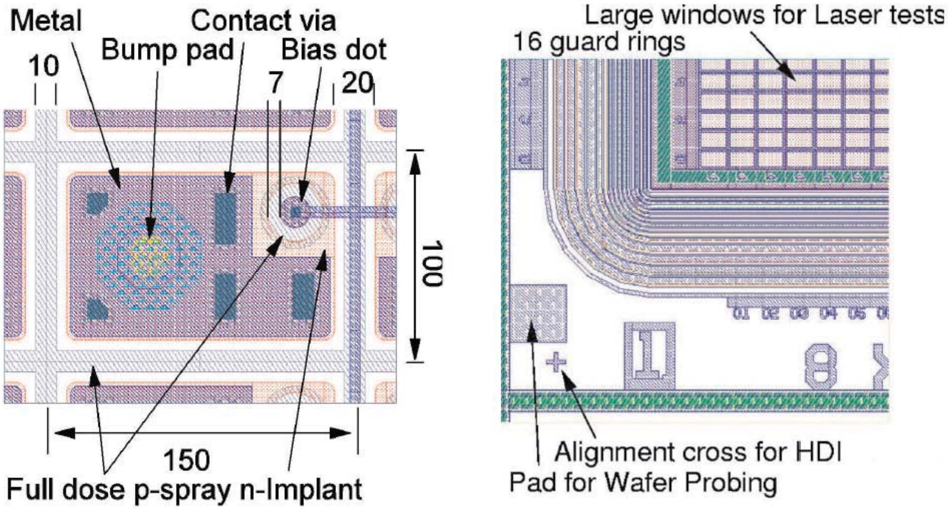


Figure 1.11. Sensor designs for the CMS barrel detector (left) and end–caps (right).

[illegible]. Dorokhov
Uni Zurich
200[illegible]

CMS barrel pixel sensor design



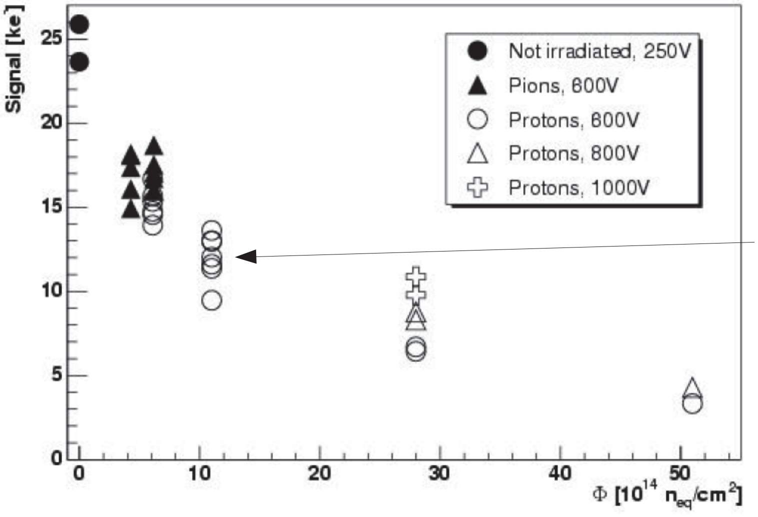
(a) (b)

Figure 1.12. The masks for the p–spray design. Left: The mask layout of the pixel side. The distances are in µm. Right: The mask layout of the backside.

T. Rohe (PSI), from A. Dorokhov (Uni Zurich) 200[illegible]

Sensor radiation damage

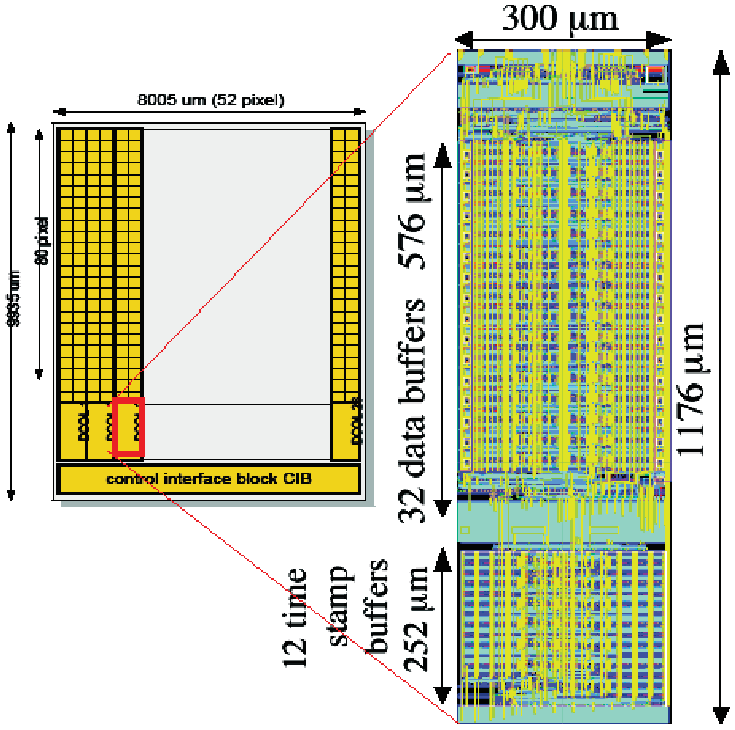
Signal collection in CMS pixel sensors



[illegible]Rohe[illegible]el[illegible]

- Inner barrel layer:
  - 70 fb^{-1} [illegible] $\times 10^{1[illegible]}$ n/cm^2
  - 2[illegible]0 fb^{-1} [illegible] 1[illegible] $\times 10^{1[illegible]}$ n/cm^2
- [illegible]0[illegible] signal loss after 2[illegible]0 fb-1.
- Also leads to factor 2 degradation of the hit resolution (less charge sharing and Lorentz angle
- Bias voltages above 600 V not possible with the present CMS HV system.
- MCz being considered.

Enlarged on-chip buffer



- **Dominant data loss mechanism → larger buffers needed**
- Data loss simulations performed
  - Data buffer from 32 to 80 cells
  - Timestamp buffer from12 to 24 cells
- Simple scaling would increase ROC size by >1.1mm
- 800 µm more space allowed with new detector mechanics
  - → Need more compact buffer layout

Enlarged on-chip buffer

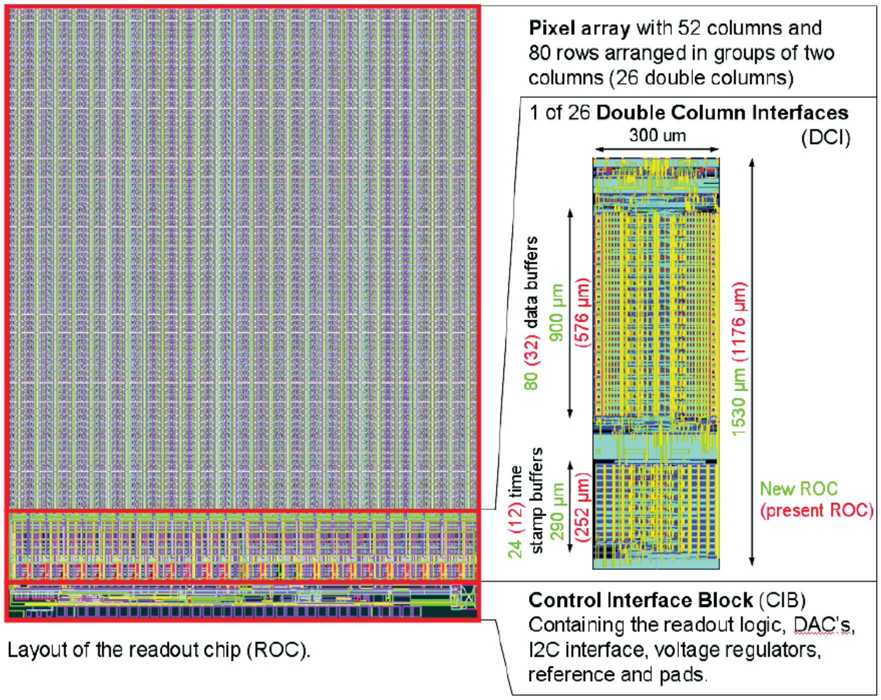


Figure 1. Layout of the existing readout chip (ROC). A detailed view of the double column interface with size of the new chip compared to the old one.

B. Meier (PSI)
Nov 2010
JINST 6 C01011

Karlsruhe and Aachen

- Karlsruhe:
  - Ulrich Husemann, Thomas Müller, professors
  - Marc Weber, professor, director IPE
  - Thomas Blank, staff IVT
  - Michele Caselle, Alexander Dierlamm, Frank Hartmann, Thomas Weiler, staff
  - Stefan Heindl, phd student
  - Tobias Barvich, technical support
- Aachen:
  - Lutz Feld, professor
  - Katja Klein, staff
  - Jan Sammet, phd student
  - technical support

□□ □t□erla□□

- Roland Horisberger, Wolfram Erdmann, Hans-Christian Kästli, Tilman Rohe, Beat Meier, Silvan Streuli, Willi Ertl, Urs Langenegger, Danek Kotlinski
- Rainer Wallny, Andrei Starodumov
- Peter Robmann