

# Vertex Detector System Design

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We describe system design issues in vertex detector design for the ILC. Meeting ILC physics goals mandates a vertex detector of unprecedented precision. Machine characteristics define the range of operational parameters. We discuss how the ILC environment effects choices in mechanical design, cooling, power engineering, and how sensor technology is affected by and affects these choices.

## 1 Physics Requirements

The ILC is designed to explore precision physics produced with low cross sections. A flagship study at the ILC will be the measurements of Higgs couplings to quarks and bosons. These measurements, which will span more than two orders of magnitude in mass and coupling strength, require excellent separation of  $b$ ,  $c$ , and light quark vertices. A related measurement is the self-coupling of the Higgs. Here the signal reaction,  $e^+e^- \rightarrow Z^0 H^0 H^0 \rightarrow qqbbbb$  with four  $b$ -jets must be separated from backgrounds like  $tt \rightarrow bbcscs$ ,  $ZZZ$ , and  $ZZH$ . Different constraints on the vertex detector come from measurements like heavy quark forward-backward asymmetry. Here the emphasis is on forward tracking with flavor tagging and determination of the charge of the parent  $b$  quark. Whether the ultimate focus is on Higgs, supersymmetry, or other new physics phenomena, it is likely that precise measurements of heavy quark jets and their decay vertices will play a crucial role [2].

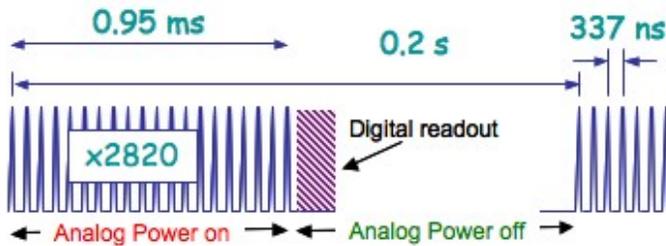


Figure 1: ILC bunch timing including possible readout and power cycling options.

## 2 The ILC Environment.

Figure 1 shows the bunch structure anticipated for the ILC, 2820 beam crossings, each separated by 337 ns are followed by a 199 ms inter-train gap. The low event rate and moderate background allow a variety of strategies to be considered to optimize the vertex detector. The long gap raises the possibility of detector readout during the gap, rather than in the train. The low duty factor means that the average power can be reduced by cycling power off between bunch trains, reducing mass needed for cooling.

The primary constraint on the geometrical design of the vertex detector is imposed by the electromagnetic background associated with the beam-beam interaction. Each crossing produces a large flux of electrons and photons caused by pair production and bremsstrahlung in the intense fields at the interaction point. Charged particles fan out of the IR in a cone whose radius depends on the central magnetic field. The requirement that the inner layer of the vertex detector avoid this cone constrains both its inner radius and length [3]. The actual background flux will depend on machine operating parameters. The level of background that is tolerable in the inner layer defines the time resolution required for the readout.

### 3 Detector Goals.

The combination of requirement for precise vertex identification and the relatively low event yield motivates a detector that optimizes the vertex information for each event. This has to be done within the constraints imposed by beam backgrounds, ILC bunch structure and integration with other components of the detector. An informal set of goals has been formulated taking these opportunities and constraints into account:

- Good angular coverage with many layers close to the interaction point
- Excellent spacepoint precision (  $< 5\mu m$  )
- Superb impact parameter resolution (  $5\mu m + 10\mu m/(p\sin^{3/2}\theta)$  )
- Low mass ( $\approx 0.1\%X_0$  per layer ). This translates to a power constraint based on gas cooling of  $< 20$  Watts in the barrel.
- Integration over  $< 150$  bunch crossings ( $45\mu sec$ )
- Electromagnetic Interference (EMI) immunity
- Moderately radiation hard ( $< 1MRad$ )

Vertex detector performance is a function of inner radius, scattering material, and detector position resolution. Figure 2 shows the results of a parametric simulation of impact parameter resolution as a function of these variables for 1 GeV tracks. The inner radius is constrained by the beam background envelope and is likely to be about 1 to 1.5 cm. Point resolutions below 5 microns have been demonstrated in several detector technologies (DEPFET, CCD, MAPs). Minimal mass is crucial for good impact parameter resolution at low momentum and, coupled with power, is a driving constraint in most designs.

### 4 Time Resolution

The time resolution required for the vertex detector depends on the machine background rate as well as the pattern recognition ambiguity tolerable in the context of the overall experiment design. Early pattern recognition studies indicated that a  $50\mu s$  integration time should be tolerable. Machine operating parameters can also play a role. For example, the first few hundred crossings in a train will be used to feedback the electron and positron beam positions to achieve head-on collisions. There is likely to be more background generated during this tuning process, which implies uneven occupancy during the train. In the absence of other

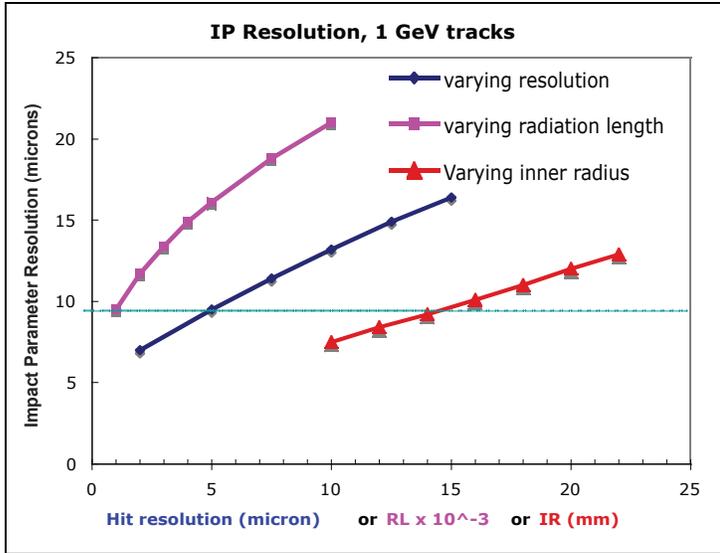


Figure 2: Parametric simulation of impact parameter resolution as a function of inner radius, detector resolution and mass using the SID geometry where the "nominal" detector (horizontal line) has  $5\mu m$  resolution, 0.1% radiation length per layer, and a 1.4 cm inner radius.

constraints shorter integration times are better. We need to understand what the tradeoffs are and what level of background is really tolerable.

There have been several approaches to achieving acceptable time resolution. For CCDs, the column parallel approach attempts to achieve 50 MHz clock rates with individual amplifiers on each column. Several CMOS MAPS devices and the DEPFET prototypes utilize a "rolling shutter" design, with a full frame readout every  $\approx 50\mu sec$ . The ISIS CCD and FAPS and CAPS CMOS MAPS devices sample charge, either in the silicon bulk or ISIS, or on external capacitors for the FAPS and CAPS devices [4] [5]. The Fermilab SOI and 3D devices [6], and the Chronopixel concept, utilize the fact that the per pixel occupancy is small during a train to store a time stamp in the pixel for each hit. This approach has the prospect of allowing crossing-level accuracy for the time stamp.

## 5 Technologies

The precision, low mass and low power required for an ILC vertex detector has driven extensive R&D on sensor technology. Each technology has features which affect any vertex detector system which utilizes them.

- CCDs - This technology was utilized for SLD, an application which bears the closest resemblance to an ILC vertex system. A standard serial readout CCD does not have sufficient time resolution to limit beam-related backgrounds. Alternative readout devices either using a column-parallel approach or in-pixel storage (ISIS) are being

pursued [7].

- CMOS Active Pixels - This technology is based on collection of charge by diffusion in the high resistivity epitaxial layer utilized in several CMOS processes. Circuits are usually limited to NMOS transistors to avoid parasitic charge collection in PMOS implants [8].
- SOI - This is a new technology which utilizes the "handle wafer", which is the base of a handle/oxide( $\approx 200nm$ )/silicon( $\approx 20nm$ ) sandwich where the sensor is formed in the handle and a full CMOS process is utilized for the top silicon. First prototypes are just becoming available from commercial vendors [9].
- 3D - This is also a new technology which utilizes vertical integration of several layers of electronics, each layer  $\approx 7$  microns thick, vertically integrated with micron-sized vias. This technology allows sophisticated processing within each pixel and the possibility of processing a field of pixels in higher tiers. The first chips utilizing this technology will be available this year [6].
- DEPFET - This technology utilizes a front-end transistor integrated into a fully depleted detector, providing both charge storage and amplification. This device can have very low noise and excellent position resolution. The current designs require readout and processing chips at the ends of columns [10].

## 6 Mechanical design

The barrel section of the ILC vertex detector is about the size of a box of Quaker Oats (in the US), about 12 cm long with a 6 cm outer radius. To meet the goal of 0.1 % radiation length per layer both the sensors and support structures must be as thin as possible. Silicon wafer thinning technology is well developed by industry, but handling these devices and keeping them flat in the face of substantial internal stresses will be a challenge. Several options are being developed. A carbon-fiber support, based on a few layers of fiber with holes to reduce mass has been prototyped by a Fermilab/Washington group. Several groups (LCFI, LBL) are experimenting with silicon carbide and reticulated vitreous carbon foam sandwich supports. Max Plank has developed a pure silicon "picture frame" support utilizing wafer bonding, thinning and etching technology.

In all of these cases a number of issues will need to be addressed before an optimal support design is available. The planarity of the sensors must be understood and whether the support structure is required to also flatten the sensors. Thermal bowing must be understood. This depends on the difference between assembly and operating temperature, which could be large for CCDs operated cryogenically. Another technology-dependent question is whether the ladder is composed of full sized single sensors (CCDs or DEPFETS) or a matrix of sensors whose size is limited to a typical CMOS optical reticle, about  $2 \times 2$  cm (SOI, 3D, MAPS).

The interconnection problem is likely to be significant. There are a number of outstanding questions that require either more work or a technology decision. Can wirebonds can be made reliably to thinned silicon without fracturing the material? What services are needed by the sensors? How much bypass capacitance is needed and where is it located? How is power coupled to the sensor and routed among sensors? What support stiffness is needed to

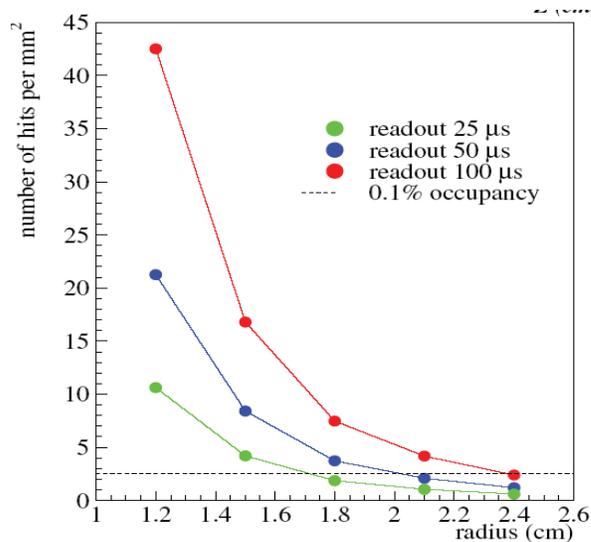


Figure 3: LDC simulation of hit density in the vertex detector as a function of radius for various integration times [11]

absorb cable torque? What independent position monitoring is needed? How would optical signals be coupled?

## 7 Power

Power considerations are likely to be the driving consideration in any vertex technology. Gas cooling is a necessity to minimize mass within the vertex detector. We can estimate the limit on total power that can be consumed by assuming laminar air flow to the vertex detector within a space that is limited by the outer tracking detectors and support structures. This has been estimated for the SiD barrel as a total of about 20 watts, or  $131\mu W/mm^2$ , with a maximum temperature rise of  $6-8^\circ C$  [12]. This is a constraint on average power, and many schemes rely on power cycling, turning on the power only during the  $1ms$  crossing period, as a way of meeting the average power constraint.

### 7.1 Technologies

Technologies are very different in their power requirements. The column parallel CCD must drive 50 MHz of capacitive clock phase lines at cryogenic temperatures. This corresponds

to about 10 amps per CCD plane. The overall power can be reduced by minimizing gate electrode capacitance or reducing clock voltages, and both schemes are being explored. ISIS-style devices, which incorporate in-pixel charge storage, can spread the power consumption throughout the 200ms cycle, reducing peak currents with respect to the column parallel design. Power for CMOS MAPS, 3D and SOI technologies are dominated by power in the front end transistors. The required power in these devices is a tradeoff between technology, speed, and noise. The thermal noise in such devices can be expressed as [13]:

$$ENC^2 = (C_{det} + C_{gate})^2 \frac{Kkt}{g_m t_s} \quad (1)$$

Where  $kt$  is the usual Boltzmann factor,  $C_{det}$  and  $C_{gate}$  are the detector load and input transistor gate capacitances,  $K$  is a constant which depends on the silicon technology (usually close to 1),  $g_m$  is the input transistor transductance, and  $t_s$  is the characteristic time of the amplifier. Pixel front end amplifiers usually operate in weak inversion where  $g_m$  is independent of device geometry and proportional to  $\frac{I_d q_e}{kt}$ , where  $I_d$  is the input transistor drain current. Noise therefore scales as  $C_{load}$  and  $\frac{1}{\sqrt{I_d}}$ .

For a power constraint of  $130\mu W/cm^2$ , with 20 micron pitch pixels, assuming a duty factor of 100 for power cycling we have a constraint of  $5.2\mu W/pixel$  or a drain current of  $3.5\mu A$  at  $1.5V$ . For a more conservative  $1\mu A$  drain current and  $100ns$  shaping time, a  $C_d$  value of 100 femtofarads (ff) gives a 35-50 electron noise level. Load capacitances of 10 ff should be achievable in SOI-based technologies, and 25-50 ff might be achievable in CMOS MAPS. Signal levels for a MAPs device with a 10 micron epitaxial layer is about 800 electrons, while a fully depleted technology like SOI or DEPFET will collect 4000 electrons in a 50 micron thick device.

## 7.2 Power Distribution

Even if we are able to meet the average power constraint for the vertex detector, we must face the issue of power distribution. For a column parallel CCD-based system we will have  $\approx 20$  modules, each utilizing 20 amps, or 4000 amps of peak clock power. A MAPS or SOI detector which meets the 20 W average barrel power constraint using power cycling will require 1333 amps of peak current if the power is delivered at 1.5 volts with a duty factor of 100. If the required voltage stability is 50 mV a 3 cm diameter copper cable is required on each side. The mass of the supply cables is unacceptable unless something is done.

The most promising technology to address cable mass is serial powering. A serial powering scheme delivers power at higher voltage, thus reducing peak currents and IR drops, enabling much lower mass cables. Each module individually regulates its voltage, passing current on to the next module at lower potential. Peak currents are reduced by a factor equal to the number of modules in series. This scheme has been tested with ATLAS strip and pixel modules and seems to work well, with no increase in overall system noise. A straw-man design for the SiD detector which includes a multiplex factor of between 9 and 15 would reduce the copper area by a factor of 12 (ignoring regulator overhead) for a given voltage drop in the supply line. The addition of the shunt/linear regulators would also relax constraints on the voltage drop allowed on the supply lines providing another large factor in the reduction of copper area.

Any power control system would have to address the rapid turn-on and off of a pulsed power system. A proper system design would probably include smart local regulation which

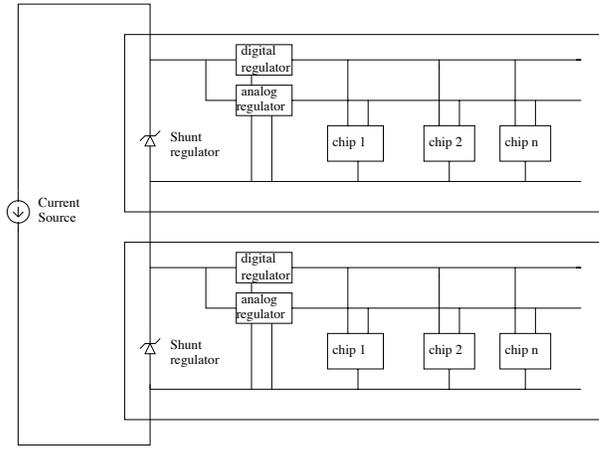


Figure 4: Schematic of a serial powering system.

could selectively depower the analog, digital, or both sections of a chip. Switching transients would have to be understood and the current supply properly synched to the detector modules to avoid overcurrent and local heating in the shunt regulator. Forces induced by the supply-return current loop have to be carefully balanced to avoid excessive torques on the low mass detector elements. Finally the mechanical and thermal effects of power switching at 5 Hz will need to be understood and carefully tested.

### 7.3 Readout Power

At the ILC essentially all hits during the bunch train will be read out. Figure 5 shows an LDC simulation of the number of hits as a function of layer for various machine operation scenarios. If we take the 1 TeV high luminosity scenario, this corresponds to a data load of  $1.4 \times 10^7$  hits per train. If we assume 30 bits per hit this corresponds to a data rate of 2 Gbit/sec. For a wire-based system the power needed would be frequency  $\times$  cable capacitance  $\times$  voltage<sup>2</sup>, or about 30 watts for 15 nf cable capacitance, saturating the power budget. Optical drivers can use much less power, the ATLAS driver utilizes  $\approx 10mW/line$ , or about 1 Watt for 96 ladders.

## 8 Electromagnetic Interference

The electron and positron beams passing the interaction region can generate substantial image currents and wakefields. These are normally shielded by the beampipe. However, if beampipe penetrations are needed for instrumentation or control, a path is available for EMI to leak out and disrupt the vertex and tracker electronics. This occurred in SLD, where the phase lock loop controlling the CCD readout dropped out of synchronization during the beam crossing [15]. This experience has led to concern about the EMI environment at ILC, with much larger beam currents.

An experiment (reported at this conference) was performed at SLAC End Station A utilizing SLC vertex electronics [16]. Antennas were placed near gaps in the beam pipe and

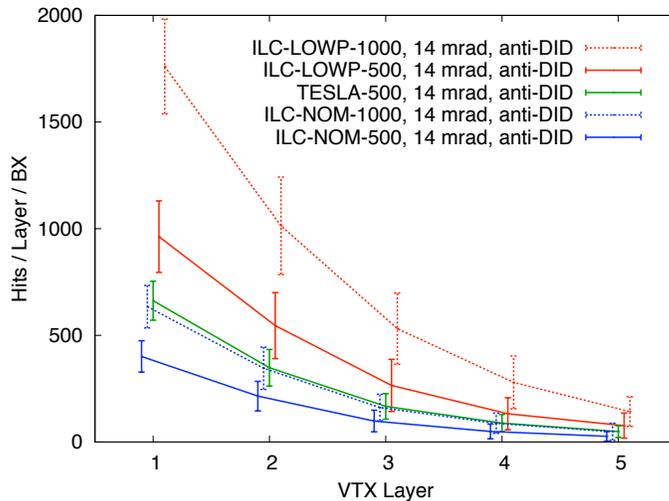


Figure 5: Vertex detector hits per beam crossing as a function of radius for various ILC operating scenarios. [14]

SLD vertex readout electronics boards were also studied. The antennas observed pulses of EMI in the high MHz range with strengths up to 20 V/m. EMI Pulse amplitudes varied in proportion to the bunch charge, and were found to be independent of the bunch length. A single layer of 5mil aluminum foil placed over the ceramic gap and clamped at both ends reduced the EMI by at least a factor of 10. A 1 cm hole in the aluminum was enough to cause the PLL to fail. These failures stopped when the hole size was reduced to .6 cm. This raises several interaction region design questions: Is there any need to have gaps in the pipe? How close to the IR would the gaps be? Can they be fully shielded? These issues need to be understood in order to understand how "EMI-hard" the vertex detector, and indeed all of the detector electronics, will have to be.

## 9 Conclusions

The ILC vertex detector presents a series of challenges to sensor technology, power control and distribution, and mechanical support. At the same time new technologies and tools are becoming available which will allow us to address the challenges. The electronics industry, in moving toward thinned wafers and 3D technology is just one example. Achieving the 0.1% layer radiation length goal will require a substantial engineering effort in understand thinned materials and supports, power cycling, power distribution, and interconnections. These items deserve a weight equal to sensor R&D.

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