

# Summary of the data acquisition session for ILC detectors

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Data acquisition is a key element for the ILC detectors. Current efforts in ongoing test-beam efforts are summarized together with future needs for the ILC. Promising new technologies like ATCA are presented as well. Please refer to the individual submissions of the DAQ session for more details and subjects that cannot be covered in this write-up.

## 1 Introduction

In the data acquisition session of the workshop, the presentations have been concentrated on two topics: DAQ systems used in current or upcoming test-beam campaigns and future needs for a 'final' ILC data acquisition system. This summary will concentrate on currently used DAQ systems by CALICE [2] and EUDET [3] and some selected topics for future DAQ systems. The expected data flow of different ILC subdetectors has been presented as well in the session, but will not be summarized in this write-up.

## 2 DAQ for current test-beam campaigns

In Europe, detector R&D efforts are currently concentrating on calorimetry, tracking and vertex detectors. The CALICE collaboration, who has recently also joined partly the EUDET activities is concentrating on developments for electromagnetic and hadronic calorimeters. EUDET is a 6th framework programme of the European Union and includes developments for vertex and tracking detectors as well as calorimetry. Because each of the subsystems has different needs, a possible harmonization between the different data acquisition systems is currently feasible only at the trigger level and/or the data level, as will be shown later.

Each of the collaborations is putting its weight to different aspects of the DAQ system. CALICE wants to get a common readout hardware for the calorimeters, aiming already for a scalable solution for later ILC detectors. EUDET on the other hand has still individual, but usually lightweight solutions for the different subgroups, but proposes a combination of different subdetector groups via a newly designed trigger logic unit. Both collaborations write their data in the LCIO data format [4] and use the GRID as a backend for storage and analysis.

### 2.1 The CALICE DAQ

Figure 1 shows a schematic overview of the hardware of the calice data acquisition system. The detector interface (DIF) is a subdetector specific component, sending the data to the link data aggregator (LDA) and from there via optical links to off detector receivers (ODRs) housed in the acquisition PCs. The CALICE DAQ aims to use as many 'off-the-shelf'

components as possible, mainly for the LDAs and the ODRs, leaving only the very front end readout and part of the DIF detector specific.

The DIFs are fed by a low jitter clock (via the LDA) and offer a bi-directional link to the LDAs. They also offer a clock feedthrough and redundant data links to neighbouring DIFs and talk to the DAQ via a standardized firmware. The LDAs have to provide a fan out for clock and control signals and a fixed latency to the DIFs. They will be developed soon and may be based on commercial Spartan-3 development boards. Data transfer from the LDAs to the ODRs is done via a commercial 16x16 optical switch from Polatis. The current ODR prototype is based on a board from PLDApplications with a Xilinx Virtex4FX60 FPGA. This prototype has demonstrated already working functionality at gigabit ethernet speeds and could be upgraded to 10G ethernet via a small daughter card.

The CALICE collaboration is still working on the presented hardware solution and expects to have a full system in a time-scale of about one year together with a custom software framework for the readout.

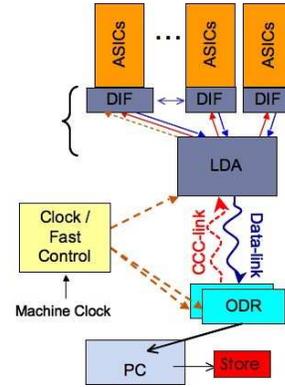


Figure 1: Schematic overview of the CALICE DAQ system

## 2.2 The DAQ for the EUDET pixel telescope

Within the EUDET collaboration, the pixel telescope working group has already performed their first test-beam activities in summer 2007. The data acquisition system of the pixel telescope is based on an adoptable readout card, the EUDRB [5], read either via VME (for test-beam activities) or USB2 (for bench-top systems). Synchronization of devices under test (DUTs) and the pixel telescope itself is achieved via a custom trigger logic unit, that has been developed by the University of Bristol [6].

Figure 2 shows an overview of the pixel telescope readout. The trigger logic unit receives inputs from the scintillators and provides a common trigger to the telescope and the DUT via LVDS signals. Optionally TTL or NIM signals are also available. DUT and telescope can synchronize either via a simple trigger/busy/reset logic or by clocking out a common event number from the TLU and attaching this number to the local events, thus avoiding any slipping of events during offline data analysis. The software framework for the pixel telescope is lightweight, platform independent (Linux, MacOSX and Windows using cygwin) and based on a minimum of open source libraries like POSIX for sockets and QT for the graphical user interface. Data is currently stored in a custom raw format for debugging reasons, but is then immediately converted to the LCIO data format and stored on the GRID for global access and analysis via 'standard' ILC software tools like Marlin etc.

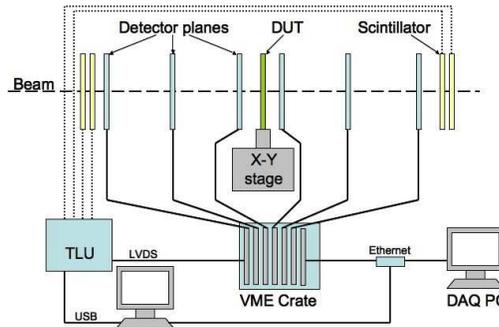


Figure 2: The EUDET pixel telescope DAQ

Within the scope of EUDET, harmonization of the DAQ will probably be done either at the trigger level, using the TLU or offline at the data level using the LCIO data format. The other subdetector groups of EUDET for tracking and calorimetry are currently evaluating the use of the TLU and external users have already successfully implemented the TLU in a combined test-beam. In the future, a common DAQ for all EUDET groups may be foreseen. Possible frameworks like ACE [7], EPICS [8] or DOOCS [9] are reviewed within EUDET, but may be implemented only in a successor program to EUDET.

### 3 ATCA, a new industry standard suitable also for ILC detectors

ATCA, or Advanced Telecom Computing Architecture is an open industry standard that has been introduced in 2005 and is supported by about 250 companies worldwide. Because of current modular standards using parallel backplanes are rapidly becoming obsolete, the HEP community needs to adapt to new platforms. ATCA is a possible candidate and first attempts to implement it are ongoing.

#### 3.1 Some features of ATCA

ATCA provides a system building block which consists of crates or shelves and 12-14 modules with vital features, like:

- dual-redundant communications node with auto-failover,
- redundant 48 V power supplies and fans,
- serial power feeds to each module, serial I/O,
- an intelligent platform manager (IPM) to diagnose and isolate faulty modules etc.,
- all modules are hot-swappable,
- crate throughput of up to 2 Tb/s, offering unlimited scalability.

All these advantages result in an extremely high availability of the system of 99.999%, resulting in down-times of less than 5 minutes per year.

#### 3.2 ATCA within the ILC scenario

The ILC will be an extremely complex machine with lots of systems and subsystems and needs a high overall availability of at least 85% [10]. As illustrated in Figure 3, this requires an availability of individual subsystems of at least 99.9%. Currently used and available technologies (VME etc.) are not able to provide this and ATCA is a valid candidate to be evaluated.

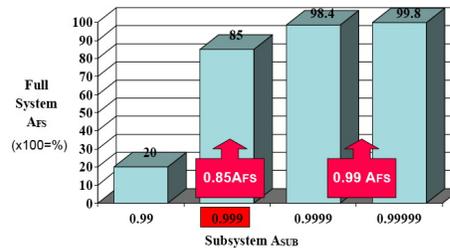


Figure 3: Required subsystem availability  $A_{sub}$  versus full system availability  $A_{FS}$ , comprising 16 systems with each 10 subsystems.

ATCA can provide off-the-shelf core components to the ILC community already today and the industry is developing the high availability software systems for the IPM etc. The offered module format is extremely versatile for custom applications, using small daughter cards on carrier boards or optional chassis sizes. Electrically, ATCA provides an excellent grounding and shielding scheme (grounding is connected in the 'right' order when hot-plugging modules) and robust connectors for multi gigabit per second serial transfer rates.

For the ILC machine, custom designs are needed. Highly precise timing and RF phase distribution modules must be built as well as specialized front-end modules for machine instrumentation. Interfaces to standard controlled machinery like movers etc. are needed and maybe also a connector system for rear transition modules (RTMs), similar to Fastbus.

Work in the ILC community has already started, with test systems at SLAC, FNAL, ANL and DESY, to evaluate the core system. DESY is currently investigating applications of ATCA for the XFEL facility and FNAL develops a 12 channel, 500 Mb/s 14 bit module for the SRF facilities. At SLAC, an ATCA to VME adaptor is under design, which will be extremely useful in the beginning for using existing readout solutions, and ANL is concentrating on system level software, interfacing to DAQ frameworks like EPICS or DOOCS.

ATCA could also be used for the ILC detectors, like for trigger systems and event building. The architecture is also valuable for inaccessible applications, but efforts must be put for radiation hard device designs, and e.g. robotic replacement for buried applications. Figure 4 shows a possible evolution from a current readout system used at LHC to an ATCA based solution, reducing drastically the amount of crates, but it needs buffering of the data close to the subdetector front-ends to profit from the architectural advantages.

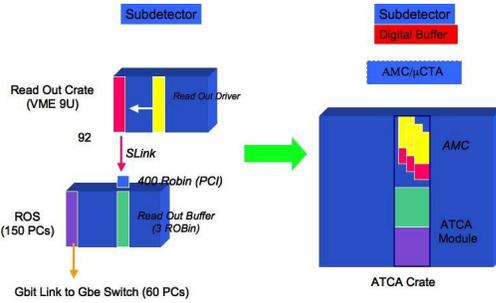


Figure 4: Evolution from a current LHC readout scheme using multiple VME crates and PCs to a possible integrated solution at ILC with a single ATCA crate.

#### 4 Future needs for the ILC DAQ

Figure 5 shows the current view of a possible uniform readout architecture for an ILC detector. Detector specific hardware and software/firmware should be integrated in the front-end of the detector and then transformed via a uniform interface. Treatment of the data should be done using commercial standards before making the data available to the worldwide global detector network (GDN). The whole is based on a 'software trigger' concept, taking into account the bunch train structure of the ILC beam. This requires up to 1 ms active pipelines for

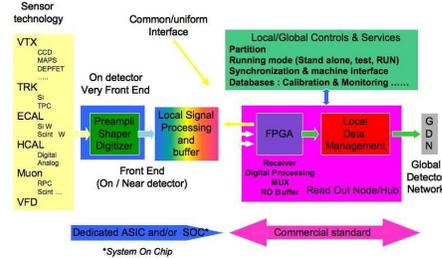


Figure 5: Current view of a uniform readout architecture for ILC detectors .

full bunch trains.

Of course, the detailed implementation still needs to be foreseen and there are remaining open questions. Do we need e.g. a trigger for cosmic rays? This has been proven extremely useful for LHC setups during installation. But because the ILC detectors will no longer be driven by external triggers, but more synchronized by a central clock, it may be difficult to implement such a scenario in individual front-end solutions. Also the details of the machine synchronization still must be worked out in the future.

## 5 Summary

The data acquisition for future detectors at the ILC is often considered to be a simple task, supposing that all the needed know-how and tools are already currently available. But already current test-beams often reach data throughputs well above recent LEP experiments and sometimes even close to LHC needs. The move from triggered machines like the LHC to a bunch-train concept like at the ILC also requires significant changes of existing DAQ schemes. Extremely high reliability of each subsystem becomes more and more important, and industrial solutions like ATCA will probably play a major role in the design of a future data acquisition system for the machine as well as the detectors at the future international linear collider.

## References

- [1] Slides:  
<http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=468&sessionId=148&confId=1296>
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- [3] <http://www.eudet.org>
- [4] <http://lcio.desy.de/>
- [5] C. Bozzi, *The data reduction board of the EUDET pixel telescope*, in these proceedings.
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- [7] <http://www.cs.wustl.edu/~schmidt/ACE.html>
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- [10] Larsen and Downing, in: Proceedings for the IEEE NSS conference, Rome, 2004.