Simulations of the Temperature Dependence of the Charge Transfer Inefficiency in a High-Speed CCD

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Results of detailed simulations of the charge transfer inefficiency of a prototype serial readout CCD chip are reported. The effect of radiation damage on the chip operating in a particle detector at high frequency at a future accelerator is studied, specifically the creation of two electron trap levels, 0.17 eV and 0.44 eV below the bottom of the conduction band. Good agreement is found between simulations using the ISE-TCAD DESSIS program and an analytical model for the former level but not for the latter. Optimum operation is predicted to be at about 250 K where the effects of the traps is minimal; this being approximately independent of readout frequency in the range 7–50 MHz. The work has been carried out within the Linear Collider Flavour Identification (LCFI) collaboration in the context of the International Linear Collider (ILC) project.

1 Introduction

Particle physicists worldwide are working on the design of a high energy collider of electrons and positrons (the International Linear Collider or ILC) which could be operational sometime around 2019. Any experiment exploiting the ILC will require a high performance vertex detector to detect and measure short-lived particles, yet be tolerant to radiation damage for its anticipated lifetime. One candidate is a set of concentric cylinders of Charge-Coupled Devices (CCDs), read out at a frequency of around 50 MHz.

It is known that CCDs suffer from both surface and bulk radiation damage. However, when considering charge transfer losses in buried channel devices only bulk traps are important. These defects create energy levels between the conduction and valence band, hence electrons may be captured by these new levels. These electrons are also emitted back to the conduction band after a certain time.

It is usual to define a Charge Transfer Inefficiency (CTI), which is the fractional loss of charge after transfer across one pixel. An initial charge Q_0 after being transported across m pixels is reduced to $Q_m = Q_0(1 - \mathrm{CTI})^m$. For CCD devices containing many pixels, CTI values around 10^{-5} are not negligible.

The CTI value depends on many parameters, some related to the trap characteristics such as: trap energy level, capture cross-section, and trap concentration (density). Operating conditions also affect the CTI as there is a strong temperature dependence on the trap emission rate and also a variation of the CTI with the readout frequency. Other factors are also relevant, for example the mean occupancy ratio of pixels (1% for a 50 MHz readout is assumed here), which influences the fraction of filled traps in the CCD transport region.

Previous studies have been reported in [1, 2, 3, 4, 5]. The novel features of this work are detailed 2D simulations using real device geometry without approximations for the charge storage volume and transport.

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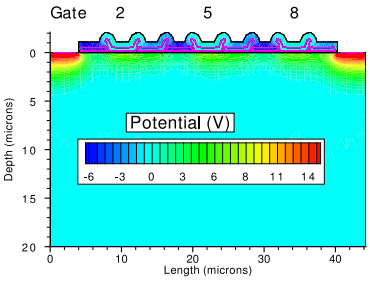

Figure 1: Detector structure and the potential under the gates after initialization. The signal charge is injected under gate 2 and is moved to the right. There are three gates for each pixel.

2 Simulations

The UK Linear Collider Flavour Identification (LCFI) collaboration [6, 7] has been studying a serial readout device produced by e2V Technologies, with a manufacturer's designation 'CCD58'. It is a 2.1 Mpixel, three-phase buried-channel CCD with 12 μm square pixels.

Simulations of a simplified model of this device have been performed with the ISE-TCAD package (version 7.5), particularly the DESSIS program (Device Simulation for Smart Integrated Systems). It contains an input gate and an output gate[a], a substrate contact and nine further gates (numbered 1 to 9) which form the pixels. Each pixel consists of 3 gates but only one pixel is important for this study—gates 5, 6 and 7. The simulation is essentially two dimensional and assumes a 1 μm device thickness (width) for calculating densities. Thus the model is equivalent to a short, thin slice of one column of CCD58 with rectangular pixels 12 μm long by 1 μm wide. The overall length and depth are 44 μm and 20 μm respectively (Fig. 1).

Parameters of interest are the readout frequency, up to 50 MHz, and the operating temperature between 120 K and 300 K although simulations have been done up to 500 K. The charge in transfer and the trapped charge are shown in Fig. 2.

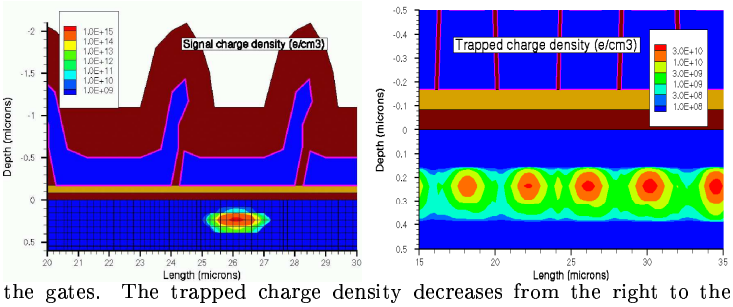

Figure 2: Left: signal charge density. The mesh size varies between 0.1 and 0.3 microns. During the analysis an integration under each gate is performed. Right: trapped charge density from transfer of signal charge at a time when the signal packet has passed under all the gates. The trapped charge density decreases from the right to the left due to emission. The time the charge spends under the gates is much longer than the time spent in the gaps (which is of the order of a nanosecond), therefore the trapped charge density is much higher under the gates in comparison with the region between the gates. The legend box refers to the region with positive depth values. At negative depth values are an oxide layer, a nitride layer, polysilicon gates and finally an oxide layer. No metal is shown.

The signal charge used in the simulation is chosen to be similar to the charge generated by a minimum ionising particle (MIP), amounting to about 1620 electron-hole pairs[b] for CCD58. DESSIS has a directive for generating heavy ions and this is exploited to create the charges. The heavy ion is made to travel in a downwards direction starting at 1.2 μm below gate 2 at 1 μs before charge transfer begins. This provides ample time for the electrons to be drawn upwards to the transport channel which is 0.25 μm beneath the gate electrodes.

[a] These separate the area under study from the input drain and output diffusion pn junctions.

[b] This number has to be divided by 12 because the charge is assumed to be distributed over the whole pixel but the model has only 1/12th of the true pixel volume.

2.1 Calculating CTI

Charge Transfer Inefficiency is a measure of the fractional loss of charge from a signal packet as it is transferred over a pixel, or three gates. After DESSIS has simulated the transfer process, a 2D integration of the trapped charge density distribution is performed independently to give a total charge under each gate. The CTI for transfer over one gate is equivalent to $CTI = \frac{e_T - e_B}{e_S}$, where e_S = number of electrons in the signal packet, e_B = number of background trapped electrons prior to signal packet transfer, e_T = number of trapped electrons under the gate, after signal transfer across gate. In this way the CTI is normalised for each gate. The determinations of the trapped charge take place for gate n when the charge packet just arrives at gate $n+1$. If the determination were made only when the packet has cleared all three gates of the pixel, trapped charge may have leaked out of the traps.[c]

The total CTI (per pixel) is determined from gates 5, 6 and 7, hence $CTI = \sum_{n=5}^{7} \frac{e_T - e_B}{e_S}$, where n is the gate number. The background charge is taken as the trapped charge under gate 1 because this gate is unaffected by the signal transport when the charge has just passed gates 5, 6 or 7.

2.2 0.17 eV and 0.44 eV traps

This CTI study, at nominal clock voltage, focuses only on the bulk traps with energies 0.17 eV and 0.44 eV below the bottom of the conduction band. These will be referred to simply as the 0.17 eV and 0.44 eV traps. An incident particle with sufficient energy is able to displace an atom from its lattice point leading eventually to a stable defect. These defects manifest themselves as energy levels between the conduction and valence band, in this case the energy levels 0.17 eV and 0.44 eV; hence electrons may be captured by these levels. The 0.17 eV trap is an oxygen vacancy defect, referred to as an A-centre defect. The 0.44 eV trap is a phosphorus-vacancy defect—an E-centre defect—that is, a result of the silicon being doped with phosphorus and a vacancy manifesting from the displacement of a silicon atom bonded with the phosphorus atom [2].

In order to determine the trap densities for use in simulations, a literature search on possible ILC radiation backgrounds and trap induction rates in silicon was undertaken. The main expected background arises from e^+e^- pairs with an average energy of 10 MeV and from neutrons (knocked out of nuclei by synchrotron radiation).

Table 1 shows results of background simulations of e^+e^- pairs generation for three proposed vertex detector designs (from three ILC detector concepts).

Simulator	SiD	LDC	GLD
CAIN/Jupiter	2.9	3.5	0.5
GuineaPig	2.3	3.0	2.0

Table 1: Simulated background results for three different detector scenarios. The values are hits per square centimetre per e^+e^- bunch crossing. SiD is the Silicon Detector Concept [8], LDC is the Large Detector Concept [9] and GLD is the Global Linear collider Detector [10].

Choosing the scenario with the highest expected background, that is the LDC concept, where the innermost layer of the vertex detector would be located 14 mm from the interaction point, one can estimate an e^+e^- flux around 3.5 hits/cm^2/bunch crossing which gives a fluence of 0.5×10^{12} e/cm^2/year. In the case of neutrons, from two independent studies, the fluence was estimated to be 10^{10} n/cm^2/year [11] and 1.6×10^{10} n/cm^2/year [12].

[c] Since some of this leaked charge might rejoin the signal packet now under the next gate, this procedure may slightly overestimate the CTI.

Particle type	0.17 eV (cm^{-3})	0.44 eV (cm^{-3})
10 MeV e^-	3.0×10^{11}	3.0×10^{10}
1 MeV n	$(4.5 \ldots 7.1) \times 10^{8}$	$(0.7 \ldots 1.1) \times 10^{10}$
total	3.0×10^{11}	4.1×10^{10}

Table 2: Estimated densities of traps after irradiation for one year. For neutrons, the literature provides two values.

$E_t - E_c$ (eV)	Type	C (cm^{-3})	σ (cm^2)
0.17	Acceptor	1×10^{11}	1×10^{-14}
0.44	Acceptor	1×10^{11}	3×10^{-15}

Table 3: Trap concentrations (densities) and electron capture cross-sections as used in the DESSIS simulations.

Based on the literature [13, 14, 15, 16, 17, 18, 19, 20, 21], the trap densities introduced by 1 MeV neutrons and 10 MeV electrons have been estimated with two established assumptions: the electron trap density is a linear function of dose, and the dose is a linear function of fluence. A summary is given in Table 2.
The actual trap concentrations and electron capture cross-sections used in the simulations are shown in Table 3.

2.3 Partially Filled Traps

Each electron trap in the semiconductor material can either be *empty* (holding no electron) or *full* (holding one electron). In order to simulate the normal operating conditions of CCD58, partial trap filling was employed in the simulation (which means that some traps are full and some are empty) because the device will transfer many charge packets during continuous operation.

In order to reflect this, even though only the transfer of a single charge packet was simulated, the following procedure was followed in all cases. During an initial 98 μs period, the gates ramp up and all the traps are filled. The gates are biased in such a way so that charge moves to the output drain. The device is then in a fully normal biased state and corresponds to the situation of a charge packet having just passed through the pixel under investigation. Since another charge packet does not arrive immediately, a 2 μs waiting time[d] is introduced before readout clocking is started. During this period some of the traps become empty. The test charge is generated 1 μs after the start of this waiting period so that 1 μs, later when the waiting ends, there is a signal packet sitting under gate 2 just at the time when the three sinusoidally varying voltages (clock phases) are applied to cause the transfer of the produced signal charge packet through the device.

3 Simulation Results

The CTI dependence on temperature and readout frequency was explored.

3.1 0.17 eV traps

Figure 3 shows the CTI for simulations with partially filled 0.17 eV traps at different frequencies for temperatures between 123 K and 260 K, with a nominal clock voltage of 7 V.

[d] This waiting time corresponds to the mean time between the arrival of charge packets from a 1% mean pixel occupancy with a 50 MHz readout frequency and to larger values for lower frequencies.

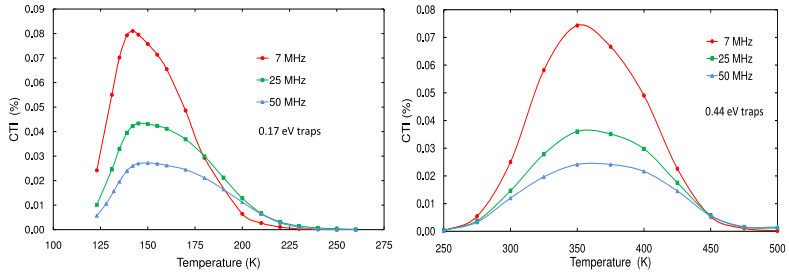

Figure 3: CTI values versus temperature for simulations with 0.17 eV (left) and 0.44 eV (right) partially filled traps at clocking frequencies 7, 25 and 50 MHz.

A peak structure can be seen. For 50 MHz, the peak is at 150 K with a CTI of 27×10^{-5}. The peak CTI is in the region between 145 K and 150 K for a 25 MHz clock frequency and with a value of about 43×10^{-5}. This is about 1.6 times bigger than the charge transfer inefficiency at 50 MHz. The peak CTI for 7 MHz occurs at about 142 K, with a maximum value of about 81×10^{-5}, an increase from the peak CTI at 50 MHz (27×10^{-5}) by a factor of about 3 and an increase from the peak CTI at 25 MHz (43×10^{-5}) by a factor of nearly 2. Thus CTI increases as frequency decreases. For higher readout frequency there is less time to trap the charge, thus the CTI is reduced. At high temperatures the emission time is so short that trapped charges rejoin the passing signal.

3.2 0.44 eV traps

Simulations were also carried out with partially filled 0.44 eV traps at temperatures ranging from 250 K to 500 K. This is because previous studies [5] on 0.44 eV traps have shown that these traps cause only a negligible CTI at temperatures lower than 250 K due to the long emission time and thus traps remain fully filled at lower temperatures. The results are also depicted in Fig. 3. The peak CTI is higher for lower frequencies with little temperature dependence of the peak position.

3.3 0.17 eV and 0.44 eV traps together

The logarithmic scale plot (Fig. 4) of the simulation results at the different frequencies and trap energies clearly identifies an optimal operating temperature of about 250 K.

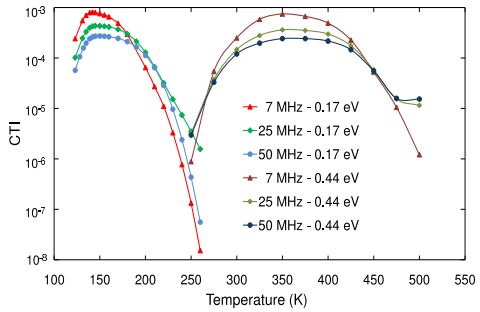

Figure 4: CTI values versus temperature for simulations for partially filled 0.17 eV and 0.44 eV traps at frequencies 7, 25 and 50 MHz (logarithmic scale).

4 Comparisons with an Analytical Model

The motivation for introducing an analytical model is to understand the underlying physics through making comparisons with the DESSIS simulations. This might then allow predictions of CTI for other CCD geometries without requiring a full simulation.

4.1 Capture and emission time constants

The charge transfer inefficiency is modelled by a differential equation in terms of the different time constants and temperature dependence of the electron capture and emission processes. In the electron capture process, electrons are captured from the signal packet and each captured electron fills a trap. This occurs at a rate determined by a capture time constant τ_c. The electron emission process is described by the emission of captured electrons from filled traps back to the conduction band, and into a second signal packet at the emission rate determined by an emission time constant τ_e.

Following the treatment by Kim [22], based on earlier work by Shockley, Read and Hall [23], a defect at an energy E_t below the bottom of the conduction band, E_c, has time constants

$$\tau_c = \frac{1}{\sigma_e \nu_{th} n_s} \qquad \tau_e = \frac{1}{\sigma_e \chi_e \nu_{th} N_c} \exp\left(\frac{E_c - E_t}{k_B T}\right) \tag{1}$$

where σ_e = electron capture cross-section, χ_e = entropy change factor by electron emission, ν_{th} = electron thermal velocity, N_c = density of states in the conduction band, k_B = Boltzmann's constant, T = absolute temperature, and n_s = density of signal charge packet. It is assumed that $\chi_e = 1$.

At low temperatures, the emission time constant τ_e can be very large and of the order of seconds. The charge shift time for one gate, $t_{sh} = 1/(3f)$, where f is the readout frequency, is of the order of nanoseconds. A larger τ_e means that a trap remains filled for much longer than the charge shift time. Further trapping of signal electrons is not possible and, consequently, CTI is small at low temperatures. A peak occurs between low and high temperatures because the CTI is also small at high temperatures. This manifests itself because, at high temperatures, the emission time constant decreases to become comparable to the charge shift time so trapped electrons rejoin their signal packet.

4.2 Charge Transfer Model

The model by Hardy et al. [24] considers the effect of a single trapping level and includes only the emission time constant in the following differential equation $\mathrm{d}n_t/\mathrm{d}t = -n_t/\tau_e$ where n_t is the density of filled traps. The traps are initially filled for this model and $\tau_c \ll t_{sh}$.

When $\tau_c \gg t_{sh}$ and to be consistent with the DESSIS simulation (that uses partially filled traps), this model can be adapted by the use of the capture time constant. The solution of this differential equation leads to an estimator of the CTI:

$$CTI = \left(1 - e^{-t_{sh}/\tau_c}\right) \frac{3N_t}{n_s} \left(e^{-t_{join}/\tau_e} - e^{-t_{emit}/\tau_e}\right) \tag{2}$$

where N_t is the density of traps, t_{emit} is the total emission time from the previous packet, the mean waiting time between charge packets related to the mean occupancy of pixels in the device, and t_{join} is the time period during which the charges can join the parent charge packet. This definition is for the CTI for a single trap level. The factor of three appears since there is a sum over the three gates that make up a pixel. (The Hardy model solution does not have the terms inside the leftmost bracket.)

Figure 5 compares the full DESSIS simulation for 0.17 eV and 0.44 eV traps and clocking frequency of 50 MHz to this Analytical Model. It emphasises the good agreement between the model and full simulations at temperatures lower than 250 K with 0.17 eV traps, but shows a disagreement at higher temperatures for the 0.44 eV traps.

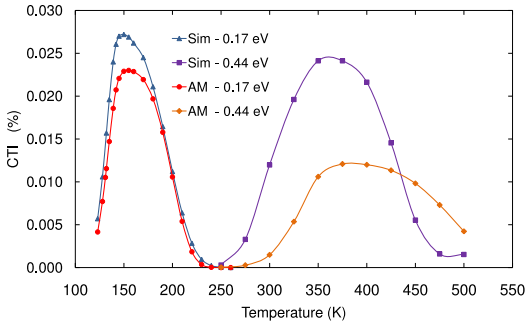

Figure 5: CTI values versus temperature for simulations for 0.17 eV and 0.44 eV partially filled traps at clocking frequency 50 MHz. Comparison of the Analytical Model (labelled AM) with the full DESSIS simulation (Sim).

However it is clear that there are limitations with the Analytical Model. They could relate to a breakdown of the assumptions at high temperatures, to ignoring the precise form of the clock voltage waveform, or to ignoring the pixel edge effects. Further studies are required.

5 Conclusions and Outlook

The Charge Transfer Inefficiency (CTI) of a CCD device has been studied with a full simulation (ISE-TCAD DESSIS) and compared with an analytical model.

Partially filled traps from the 0.17 eV and 0.44 eV trap levels have been implemented in the full simulation and variations of the CTI with respect to temperature and frequency have been analysed. The results confirm the dependence of CTI with the readout frequency. At low temperatures (< 250 K) the 0.17 eV traps dominate the CTI, whereas the 0.44 eV traps dominate at higher temperatures.

Good agreement between simulations and an Analytical Model has been found for 0.17 eV traps but not for 0.44 eV traps. This shows the limitations of the model with respect to the full simulation.

The optimum operating temperature for CCD58 in a high radiation environment is found to be about 250 K for clock frequencies in the range 7 to 50 MHz. However CCD58 is not really suited to high speed readout and attempts to make laboratory measurements have given inconsistent results. So in order to meet the demanding readout requirements for a vertex detector at the ILC, interest has now moved to an alternative CCD design with Column-Parallel (CP) and 2-phase readout. Our prototype CP-CCD has recently operated at 45 MHz. Thus our involvement with serial readout devices will probably now cease but the experience gained with DESSIS and building analytical models will transfer to our studies of CP-CCDs.

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