Development of an ILC Vertex Detector Sensor with Single Bunch Crossing Tagging[1]

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The hit density for an ILC vertex detector requires multiple hit capability within a bunch train. The ideal performance would be to associate uniquely each hit with a specific bunch crossing within the bunch train. We are developing a CMOS sensor with this capability, providing a four deep buffer per pixel to accumulate hit times during the one millisecond bunch train. The design of first prototypes for this sensor has been completed, with two buffers in 50 μm x 50 μm pixels, and devices are expected to be produced during the coming year based on 0.18 μm technology. The 4 deep buffer, with $\sim$10 μm pixel sensors are planned in a later step with 45 nm technology.

1 Introduction

A pixel vertex detector is a powerful tool for ILC experiments, capable of independent track reconstruction, as demonstrated by the 307 Mpixel CCD vertex detector at SLD.[2] The time structure of the ILC necessitates an extremely fast readout of the vertex detector elements. Monolithic CMOS pixel detectors that allow extremely fast non-sequential readout of only hit pixels have advantages over CCDs. We have initiated an R&D effort to develop such devices having time stamps with single bunch crossing precision for each hit. These "Chronopixel" detectors thereby significantly reduce the effective backgrounds relative to a sensor that integrates over many bunch crossings.

The ILC offers a unique environment in which to achieve exceptional physics goals due to the modest event rates, relative rates of background to signal, and relatively low radiation levels. Precision measurements of the branching ratios for many of the Higgs decay modes is a primary goal, and superb flavor tagging is needed to achieve this. The goal for the impact parameter resolution is $5\mu\text{m} \oplus 10\mu\text{m}/(\text{p} \sin^{3/2}\theta)$, requiring spacepoint precision of better than 4 μm. The transparency requirement is $\sim$0.1% X_0 per layer. The 3.9 μm spacepoint precision and 0.4% X_0 transparency of SLD encourages this goal.

2 Operational Constraints

The baseline time structure of the ILC results from bunchtrains of 2820 bunches spaced 337 nanosecconds, passing through the collider hall 5 times a second. Consequently, each bunch train is about 1 msec long, with about 200 msec between bunch trains.

In general, the requirements for the sensor are:

1. Good angular coverage with several layers close to the interaction point;

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2. Excellent spacepoint precision (< 4 μm);
3. Superb impact parameter resolution;
4. Transparency ($\sim 0.1\%$ X_0 per layer);
5. Track reconstruction (in VXD alone);
6. Low occupancy ($< 10^{-3}$ hits/pixel);
7. EMI immunity; and
8. Power constraint (< 100 Watts for the entire vertex detector).

3 Progress on Monolithic CMOS Pixel Detector Design

During the past three years a conceptual design for a monolithic CMOS device that should meet the ILC vertex detector requirements has been developed by Oregon and Yale in collaboration with the Sarnoff Corporation[3] through an R&D contract. In this design each pixel (smaller than 15 μm $\times 15\mu$m) contains electronics to store the bunch number (time) of up to four hits above an adjustable threshold (thus "Chronopixels"). Hits are read out during the 199 msec between bunch trains. The pixels can achieve up to 3 to 4 micron precision without analog information. A simplified schematic of the in channel electronics design is shown in Figure 1.

3.1 General Description of the Design

The system design includes sensors up to 12.5 cm $\times$2.2 cm with 10 μm $\times 10\mu$m pixels. This is achieved with pixel electronics within each pixel area, on the same piece of silicon (monolithic CMOS) thinned to a thickness of 50 to 100 μm. The electronics for each pixel records hits above an adjustable threshold. The time of each hit is stored in each pixel, up to a total of four hit times per pixel, with single bunch crossing precision (thus the name "Chronopixels" for this device). Hits will accumulate for the 2820 bunch crossings of a bunch train and the sensor is read out during the 200 msec between bunch trains. Only the coordinates (x,y,t) for hit pixels are read out. With 10 micron size pixels analog information is not needed to reach a 3 to 4 micron precision; only digital readout is planned, considerably simplifying the electronics.

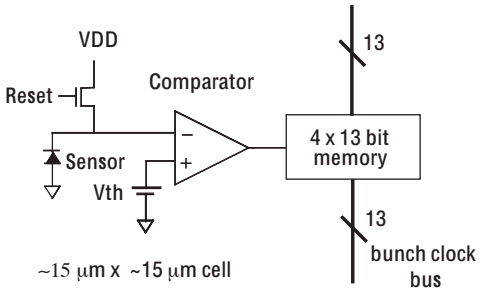

Figure 1: Pixel Architecture

Extensive background calculations[4] indicate that the maximum total hit rate in the innermost layer of the vertex detector will be 0.03 hits/mm^2/bunch crossing. With 2500 mm^2 per sensor (a total of 25×10^6 pixels) and 2820 bunch crossings per train we expect 2×10^5 hits/sensor/bunch train, or an occupancy of the order of one percent in these inner layers. This appears much too high to allow efficient pattern recognition. The crucial element of our design is the availability of the time information (i.e., bunch crossing number) with each hit. An event of interest at a known time in a subsystem, such as the tracker or calorimeter, are associated with vertex detector hits in time, and the occupancy is $< 10^{-5}$ per pixel (SLD worked well with a vertex detector occupancy of 10^{-3} per pixel).

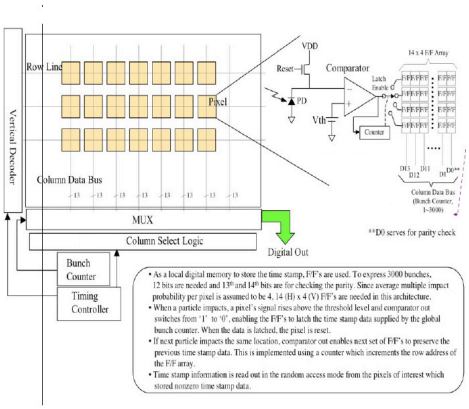

Figure 2: Chronopixel Array Architecture

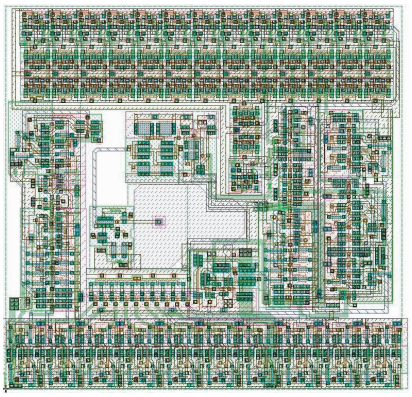

Figure 3: Image of the 645 transistor pixel design

3.2 Detailed Design

SARNOFF has designed the electronics under each pixel of the Chronopixel array, shown schematically in Figure 2. The functionality of this design has been verified by an hspice simulation.

The analog components of the circuit (the boxes labeled Detector and Comparator on Figure 2) are estimated to consume most of the power, $\sim$15 milliwatts/mm^2. The remaining digital components are estimated to be around 0.05 milliwatts/mm^2. The analog components are only needed during the time when hits are accumulated during the bunch train, $\sim$1 msec. The average power can thus be reduced by a factor of $\sim$100 by turning off the analog parts during the 200 msec digital readout. This reduces the average power consumption to the vicinity of 0.5 watts per sensor or to the order of 100 watts for the vertex detector, which seems acceptable.

During the last year Sarnoff completed the design of the first prototype device. Using a TSMC 0.18 micron process they were able fit the circuitry needed for each pixel into a area slightly larger than $50\,\mu$ by $50\,m\mu$. An image of this design is shown in Figure 3. This design is complete and is awaiting LCDRD funding for production. As the purpose of the design is to test the pixel circuitry, the pixel has been designed to use a standard TSMC process and will not be active over the entire $50\,\mu$m by $50\,\mu$m area.

The circuitry in the pixels has been carefully designed to be scalable to smaller features sizes. To achieve a pixel that is $\sim 10\,\mu$m by $\sim 10\,\mu$m a smaller feature size CMOS, e.g. 45nm, will be used.

We produced a detailed simulation of the pixel active area and has investigated the ultimate pixel geometry which will need a process with a smaller feature size than 0.18 microns, a thick epitaxial layer and a deep-p well. As this will eventually require an expensive custom processes, we are presently concentrating on a proof of concept run with a standard

TSMC process.

3.3 Discussion

Readout Scheme Each sensor will consist of 2000 columns with 12500 pixels per column, divided into 40 readout regions of 50 columns each. At the end of the bunch train, when the electromagnetic interference due to the beam has died off, the 40 regions will be read out in parallel at 25 MHz into a FIFO buffer located at the end of each sensor. The contents of the FIFO buffer will be read out at 1 GHz. We thus expect to read out the full sensor (2×10^5 hits, with 38 bits per hit) in about 8 msec. This leaves a safety margin of 25 with the 200 msec gap between trains.

Charge Spreading. In order to optimize digital readout, charge spreading should be contained within the pixel volume. This is accomplished by maximizing the depletion depth, and benefiting from the effects of small stray fields extending into the undepleted region The design depletes the charge sensitive epitaxial layer to the maximum extent possible. Employing the highest feasible silicon resistivity is important. Our detailed simulations of the chronopixel design indicate that full depletion of the epilayer is not possible. We will rely on the field extension into deep portions of the epilayer volume to constrain the drift of charge. Our simulations model this field, and the resulting drift.

Charge Statistics and Read Noise. A Monte Carlo calculation indicates that a 1 GeV pion at normal incidence has a most probable yield of 800 electrons for a 15 micron thick charge sensitive epitaxial layer.[5] The designed read noise is 25 electrons; if this is achieved in the prototype, it comfortably achieves the required signal to noise for high efficiency particle detection with low backgrounds. Two strategies are employed to achive this low noise performance. A soft reset[6] is used, as well as a negative feedback circuit.

References

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