CALICE-DAQ communication and DAQ software

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This note describes work on the data acquisition system for a calorimeter of the future International Linear Collider (ILC) within the CALICE collaboration. Focus is on options for the network, requirements of the clock, a potential bottle neck for the control data and a use case analysis of the software for the data acquisition system.

1 Introduction

The planned data acquisition system is developed within the EUDET project which is scalable to the data rates which will occur in the final calorimeter and therefore give input to the Technical Design Report of one of the detectors. The work is carried out within the CALICE-UK groups.

The current design of the data acquisition (DAQ) system distinguishes between the very front-end electronics (VFE), which is located on the detection slabs and consists of ASICs, and the front-end electronics (FE),which is located at the end of the detection slab and consists of a FPGA and control systems. The closest part of the FE to the VFE is the detector interface (DIF) which has to be customized to the choice of the detector type and the VFE choices. The DIF translates the data into a common format. Therefore any other FE component is independent of the choices of the detection layer. Several DIFs are connected to a link data aggregator (LDA) which sends the data over an optical link to the off detector receiver (ODR). The ODR is a PCI (Peripheral Component Interconnect) card within a DAQ PC from where the data will be saved to disk. It is estimated that the total data volume to be read out from the calorimeter is about 5 Gb or about 1 Mb per slab for one bunch train, i.e. about 5 Mb/s for a slab.

2 Network and Switching

Between the LDA and the ODR a fast network of optical cables is envisaged. In order to reduce the overall cost of the hardware the work on the network is focussed on testing options for a 10 Gb/s network. On the ODR side it has been successfully shown that high bandwidth usage of over 9 Gb/s using PCIe 10Gig cards from Myricom [1] can be performed. Tests with multiple 10 Gb/s transfers are ongoing. To simulate data transfers from the LDA to the ODR a FPGA based Ethernet system using RAW frames has been setup and successfully tested with bi-directional communications in a request-response mode. The plan is to study multiple receivers talking to more than one FPGA system.

The performance of dispatching and routing tasks of a network switch between the LDA and the ODR is investigated. The motivation is to have high data-taking efficiency. Because the transport format of the data needs to be customized in order to allow for clock and control data to be uploaded to the slab an optical switch needs to be used. A 16x16 fibre multi mode optical switch has been purchased from Polatis [2].

3 Clock

It is understood that a machine clock will be used which will be fed into the ODRs. The clock will then be distributed to the LDAs which then distributes the clock to the DIFs. In turn the DIFs distribute the clock to the VFE. For debugging and test purposes an interface of the machine clock to the LDAs and the DIFs needs to be introduced. A couple of constraints on the clock have been identified:

- The machine clock will be running at a frequency around 50 MHz with low jitter. The fast commands will be accurate to a period of the machine clock. This requires a fixed latency in the command channel.
- The ODR needs to be running on a frequency of 125 MHz due to the link specifications of the optical link connection between the ODR and the LDA.
- The LDA derives the machine clock with low jitter. It is estimated that a jitter less than 1 ns is needed for the detectors.
- The bunch spacing is about 320 ns which corresponds to 3.125 MHz. Therefore at the DIF the machine clock needs to be divided by a factor 16. Due to the long time between bunch trains it would be helpful to have a fast command which determines the bunch clock phase with respect to the machine clock.

4 Single Event Upset

A study of single event upsets (SEUs) is part of the study of the configuration data which need to be send to the FE. The study tries to identify bottle necks which could arise. SEUs can occur in the electronics if a particle (typically a neutron, proton or pion above a certain threshold energy about 20 MeV) traverses the electronics and generates enough electron-hole pairs in the active area of the silicon material such that a change in the state of the circuit occurs. Typically these changes can be reset in FPGAs and therefore SEUs do not lead to permanent damage. However in order to reset the FPGAs at a reasonable rate one needs to know the rate at which SEUs occur.

For this study detector simulations using PYTHIA and MOKKA with the TESLA design have been performed for physics events which occur frequently according to the TESLA TDR [3]. In this study WW, QCD and $t\bar{t}$ events were simulated. The particle spectra of particles traversing the ECAL front-end electronics were generated. It was shown that all of these simulations were dominated by QCD events.

It has been shown that the SEU rate arising from physics events with today's FPGAs lies in the area to several days for today's FPGAs in the TESLA ECAL. Thus requiring the FPGAs in the ECAL to be reset at a higher rate to mitigate these effects. It needs to be noted that this study only comprises physics events. The machine background has only been studied partially up to now.

The occupancy resulting from physics events of the ECAL barrel could be determined from the simulations. It is estimated to be $5{\times}10^{-4}$ per bunch train for physics events. The

occupancy is expected that this number will rise when you consider the machine background and noise. A linear collider note describing the study in more detail and adding radiation backgrounds is under development.

5 DAQ software

The requirements of the DAQ software for the technical calorimeter prototype within the EUDET project are currently discussed and use cases have been constructed. From the use cases it became clear that a state machine for the start and the close down of the DAQ needs to be used. The transitions need to take into account to check the status and the communication of the system, the configurations need to be distributed to the VFE before any data can be taken. It also needs to be noted that all of the checks and distributions of configurations need to be saved in a book keeping database.

A point of discussion is how to store the data. This depends on the data rate. Three scenarios have been envisaged: For data rates up to 200 Mb/s the data can be sent from a local disk on the DAQ PC to a central storage; for higher data rates a RAID array needs to be used; for data rates higher than about 1600 Mb/s the data can not be locally stored any more, but needs to be transferred in memory. Thus increasing the risk of failure of the data transfer. For the EUDET prototype an estimate has been made that the data rates of the DAQ will be about 400 Mb/s, however heavily depending on the detector and VFE choices.

6 Conclusion

In this note the design and development undertaken for the ILC calorimeter DAQ is presented. Special emphasis is put on the network, clock and configuration data as well as on the DAQ software. The ongoing research to provide a 10 Gb/s link solutions and an optical switch are described. The requirements for a clock system are discussed. An estimate for SEU rates deriving from physics events within the FE is given which is between about 40 days in the electromagnetic calorimeter of TESLA design. Concepts of use cases and the state machine for the DAQ software are discussed with the help of which a DAQ software will be designed.

References

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