Readout electronics for LumiCal detector

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The readout electronics for the luminosity detector (LumiCal) at ILC is discussed. First, the challenges of LumiCal and the proposed solutions are described together with the overall readout architecture chosen. Then a more detailed description of the front-end and the analog to digital convertion blocks follows. In particular the design and simulation results of the prototype preamplifier, shaper and basic ADC blocks are presented.

1 Introduction

The project of LumiCal readout electronics depends on several assumptions concerning detector architecture. At present development stage it is assumed that the LumiCal detector is built of 30 layers of 300 μm thick DC-coupled silicon sensors whereas each layer is divided into 48 azimuthal sectors. Each sector, with the inner radius of 8 cm and the outer of 35 cm, is segmented into 96 radial strips with a constant pitch. Such design results in very wide range of sensor capacitance which will be connected to the front-end. The LumiCal readout should work in two modes: the physics mode and the calibration mode. In physics mode the detector should be sensitive to electromagnetic showers of high energy deposition (up to about 15 pC of ionized charge) in a single sensor. In calibration mode it should detect signals from relativistic muons, i.e. it should be able to register the minimum ionizing particles (MIPs). Because of very high occupancy expected the front-end electronics should resolve signals from particles in subsequent beam bunches and so should be very fast. The requirements on power dissipation can be strongly relaxed if a total or partial power supply switching off is applied in the periods between the bunch trains.

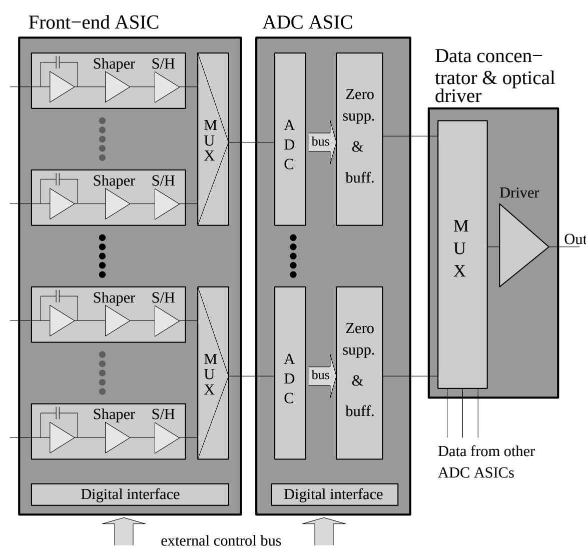

Figure 1: Block diagram of the LumiCal readout electronics

To fulfill all the reqirements the general concept of the readout electronics was outlined as shown in fig. 1. The main blocks in the signal flow are: the front-end electronics, the A/D conversion plus zero suppression and the data concentrator with optical driver. The first two blocks of fig. 1, i.e. the front-end and the ADC need to be designed as dedicated multichannel ASICs. In the following the designs of these blocks are discussed and simulation results are presented [1]. The data concentrator and optical driver block will be studied on further development stage. The prototype designs of discussed ASICs are done using the AMS 0.35μm technology.

2 Front-end electronics

The front-end electronics detect signals from silicon sensor, amplify and shape them in order to obtain the required signal to noise ratio and finally sample and store their amplitudes. The memorized amplitudes are sent to an A/D conversion block. These operations are done in parallel in all channels of the front-end ASIC. The features of LumiCal already mentioned set important constraints and requirements on the front-end. They concern mainly the wide input capacitance range 10-100 pF per channel, the wide range of charge 2 fC-15 pC deposited in a single sensor and the high speed (pulse duration of about 360 ns). The low noise requirements are driven by calibration mode operation where a S/N ratio of about 10 should be sustained even for the largest sensor capacitance. At present stage the power dissipation per channel is constrained to 10 mW. In order to fulfill the requirements concerning low noise operation and wide range of input capacitance a charge sensitive preamplifier configuration was chosen. Two architectures of front-end using this configuration are currently under study: one with continuous pulse shaping and other based on Switched-Reset scheme. Both architectures with simulation results are discussed below. The sample and hold circuit (S/H) and the multiplexer circuit (MUX) are not discussed here since they have not been designed yet.

2.1 Front-end with continuous pulse shaping

Each front-end channel is built of the preamplifier, pole-zero cancellation circuit (PZC) and shaper as shown in fig. 2. The preamplifier integrates the signal from a sensor on the feedback capacitance. The PZC circuit is used in order to shorten a slow tail of the preamplifier response and in this way to improve high input rate performance. To optimize the signal to noise ratio and high speed performance the preamplifier and PZC is followed by a pseudo-gaussian shaper with a peaking time of about 70 ns.

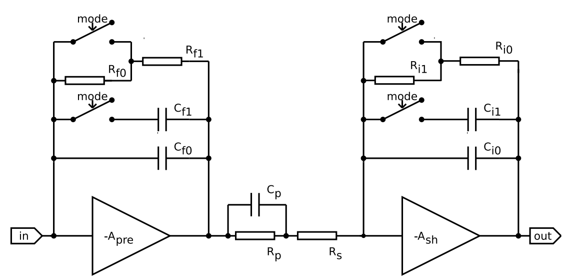

Figure 2: Schematic of preamplifier, PZC and shaper. Switches set to calibration mode

In order to cover the amplitude range of input signals, from MIPs in the calibration mode to more than 10 pC in the physics mode a variable gain scheme is implemented. The gain control is realized by the switches in the preamplifier and shaper feedback. As can be easily calculated the transfer function of circuit in fig. 2 is equivalent to a standard CR-RC first order shaping. Both the preamplifier and shaper circuits are designed as folded cascodes with active loads, which are followed by buffers.

The front-end is designed as a multichannel ASIC. In order to match the sensor segmentation a single ASIC containing 32, 48 or 64 channels is considered for the final version.

Simulations of the proposed front-end were done using Cadence package with Hspice and Spectre simulators. The typical simulated responses for sensor capacitances in the range 10-100 pF are shown in fig. 3 for the calibration mode (mode0) and for the physics mode (mode1). One can notice that in the calibration mode the amplitude and peaking time depend on input capacitance. This happens because in the calibration mode, where the preamplifier's feedback capacitance C_f is small ($\sim 400fF$), the ratio of the sensor capacitance C_{det} to the effective input capacitance $C_{eff} \simeq A_{pre} \cdot C_f$ is not negligible since the preamplifier gain A_{pre} is below 1000 while the sensor capacitance reaches 100 pF. In such case some part of input charge is lost on sensor capacitance and the preamplifier can not be considered as purely charge sensitive. On the contrary, in the physics mode where the feedback capacitance is large ($\sim 10\ pF$) the aforementioned ratio may be neglected and the preamplifier behaves as charge sensitive. This is seen in fig. 3 (mode1) where the dependence on input capacitance is hardly noticeable. The simulations were done for a wide range of input charge. The circut is linear up to about 7 pC and fully saturates above 15 pC. In all simulated cases the S/N ratio stays above 10.

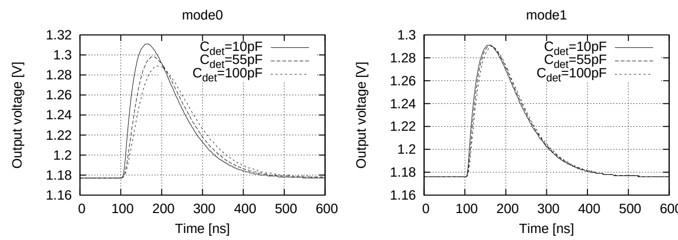

Figure 3: Example of shaper output in calibration mode for 10fC input charge (mode0) and in physics mode for 1pC input charge (mode1)

2.2 Switched-Reset front-end

The preamplifier with feedback reset instead of feedback resistance could be a very atractive configuration because such solution does not need a shaper and has large output dynamic range. For this reason a charge sensitive configuration equipped with reset switch as shown in fig. 4 is also investigated. The preamplifier is designed as a folded cascode. To allow variable gain operation different values of feedback capacitances are implemented. The calibration mode configuration is obtained using the smallest capacitance C_{f0}. Simulations of this configuration were performed for a wide range of input capacitancies and input charges. In all cases signal risetime is below 300 ns. Since the simulated reset time of the preamplifier never exceeds 40 ns the full cycle of pulse response and the reset can be kept between two bunches. In the calibration mode the circuit is linear up to about 300 fC and saturates for higher input charges. In the physics mode the linearity region can be extended to tens of pC by increasing the feedback

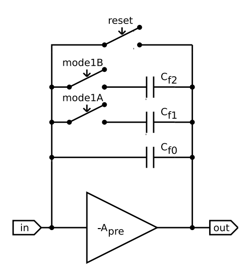

Figure 4: Schematic of switched-reset preamplifier

capacitance. The circuit noise performance is currently under study.

3 Analog to Digital conversion

In the LumiCal detector the energy deposited in a sensor, detected and amplified in the front-end electronics, needs to be digitized and registered for further analysis. This is done in the ADC and zero suppression block. Simulations of LumiCal indicate that the reconstruction procedure needs about 10 bit precision on the measurement of deposited energy. Considering the number of detector channels needed and the limitations on area and power, the best choice for the analog to digital conversion seems a dedicated multichannel ADC. To save the area a reasonable solution is to make one faster ADC for 8 channels of the front-end electronics. Since the LumiCal detector requires a sampling rate of about 3 MHz per channel an ADC should sample the data with at least 24 MHz rate. On the other hand a single 3 MHz ADC per each channel would be the simplest solution from the designer point of view. Both solutions are still under consideration.

One of the most efficient architecture assuring a good compromise between the speed, area and power consumption is a pipeline ADC, and this architecture was chosen for the LumiCal data conversion. Below, the design of main blocks of pipeline ADC is briefly described. The part of ADC block responsible for zero suppression is not discussed here since it is not implemented yet.

3.1 ADC Architecture

Pipeline ADC is built of several serially connected stages as shown in fig. 5. In the proposed solution a *1.5 bit stage* architecture was chosen because of its simplicity and immunity to the offsets in the comparator and amplifier circuits. Since single stage generates only three different values coded on 2 bits it is called *1.5 bit stage*. Each stage from fig. 5 generates 2 bits which are sent to digital correction block. In the correction block 18 output bits from 9 stages are combined together resulting in 10 bits of ADC output.

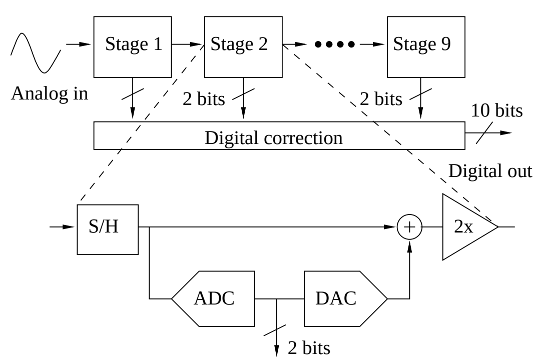

Figure 5: Pipeline ADC architecture

The block diagram of a single stage is shown in fig. 6. Each *1.5 bit stage* consist of two comparators, two pairs of capacitors C_s and C_f, an operational transconductance amplifier, several switches and small digital logic circuit. To improve the ADC immunity to digital crosstalks and other disturbances a fully differential archutecture is used. The operation of the stage is performed in two phases. In phase φ_1 capacitors C_s and C_f connected to ground through S_1(in reality to common voltage, ground is used in description only for simplicity) are charged to voltages $V_{i\pm}$. In phase φ_2 the switches S_2 and S_3 change positions and S_1 is open. The C_f are now in the amplifier feedback while the C_s are connected to DAC reference voltages ($\pm V_{ref}$ or 0 depending on comparators decision). In the *1.5 bit stage* architecture $C_f = C_s$ is chosen to obtain a gain of two in the transfer function.

The critical block of pipeline ADC is the fully differential amplifier. A telescopic cascode amplifier configuration is used here since it represents the most efficient solution with respect to speed vs power. In order to obtain high enough gain (of about 80 dB) required for 10 bit resolution a gain boosting amplifiers are used in both upper and lower cascode branches. Since the *1.5 bit stage* architecture leaves very relaxed requirements on the comparators (~100mV treshold precision) a simple dynamic latch architecture was chosen. For the present prototype all reference voltages are assumed to be applied externally.

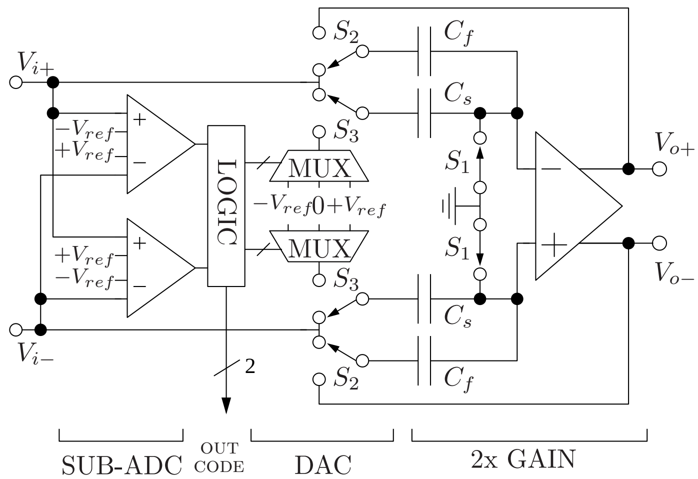

Figure 6: Simplified schematic of a 1.5 bit stage. Switches set to φ_1 phase

4 Summary

To sumarize it should be stressed that the work on the LumiCal readout electronics has just started. The main readout circuits i.e. the front-end and the ADC are being simulated and first prototypes are submitted. In the next evaluation stage the sub-circuits not yet designed like sample and hold (S/H) or multiplexer (MUX) will be integrated and prototyped as well. Then the integration of multichannel ASICs with all channels and full functionality comprising all necessary controls, DACs, zero suppression etc. will be added.

Acknowledgments

This work was partially supported by the Commission of the European Communities under the 6^{th} Framework Programme "Structuring the European Research Area", contract number RII3-026126.

References

[1] Slides:
`http://ilcagenda.linearcollider.org/contributionDisplay.py?contribId=390&sessionId=108&confId=1296`