Study of Readout Electronics for LumiCal detector

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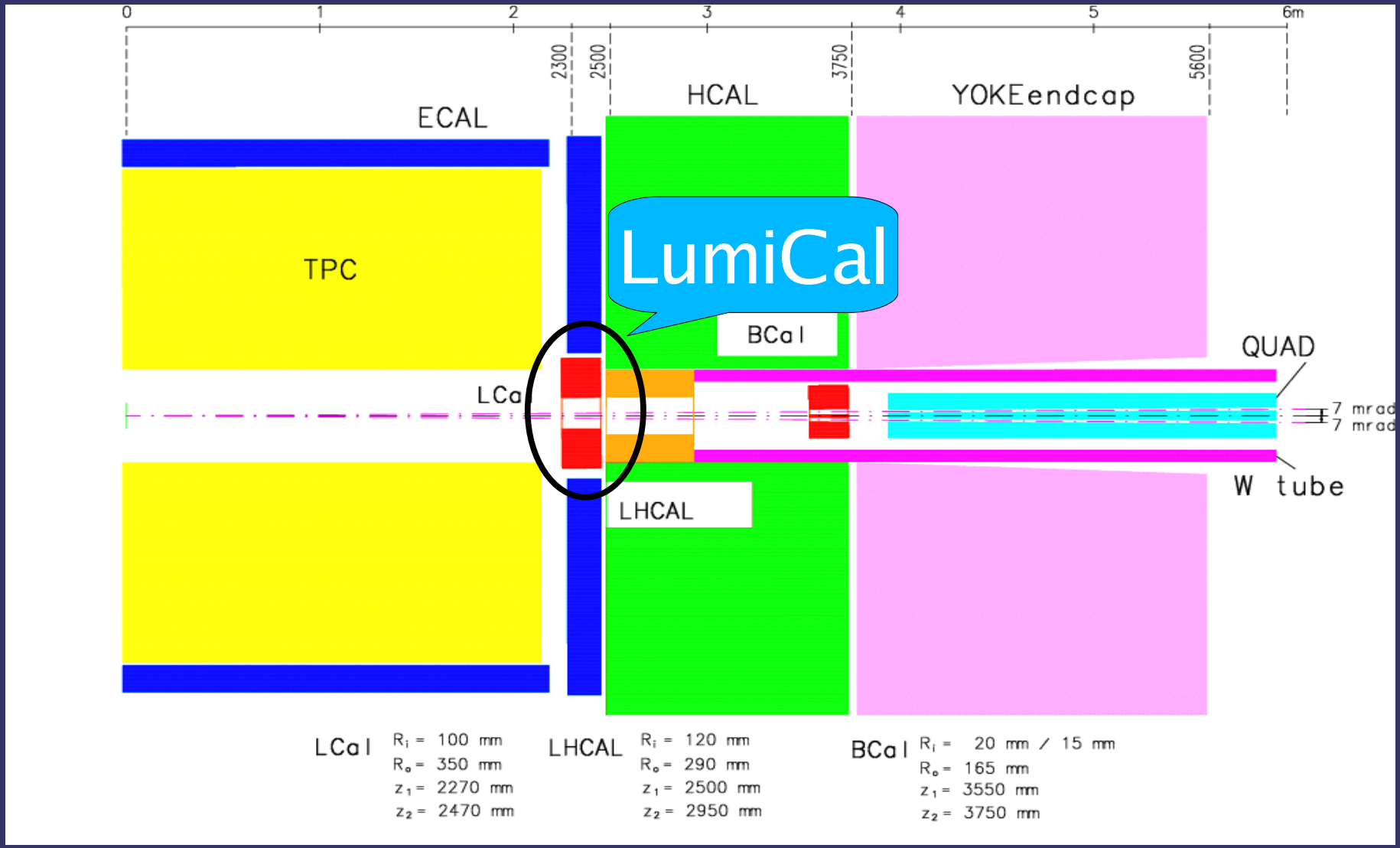
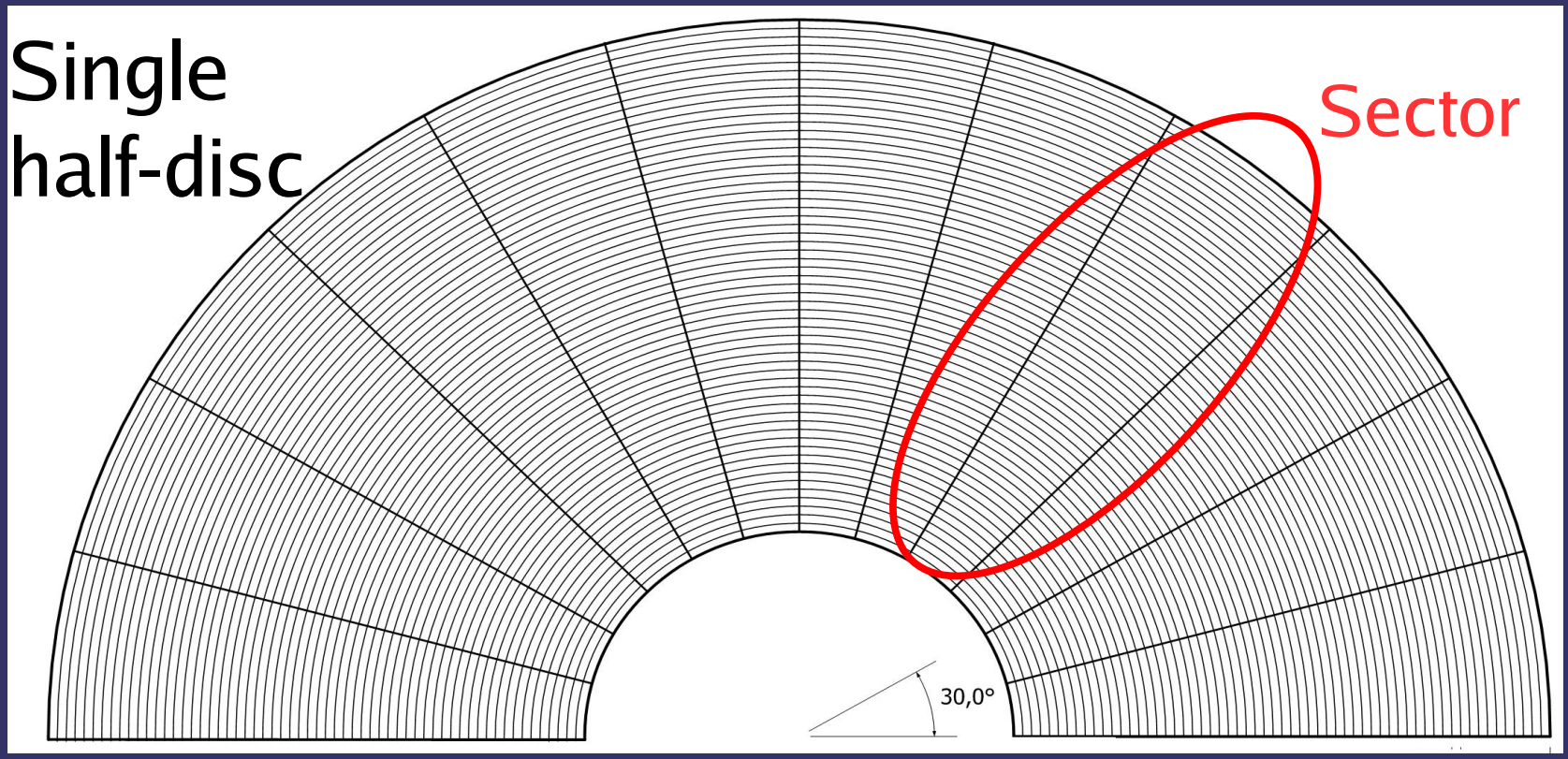
Outline

- LumiCal detector overview
- Specifications & implications for front-end
- Noise considerations - theory
- Front-end design & preliminary simulations
- Overall readout architecture
- Summary & Schedule

General detector architecture



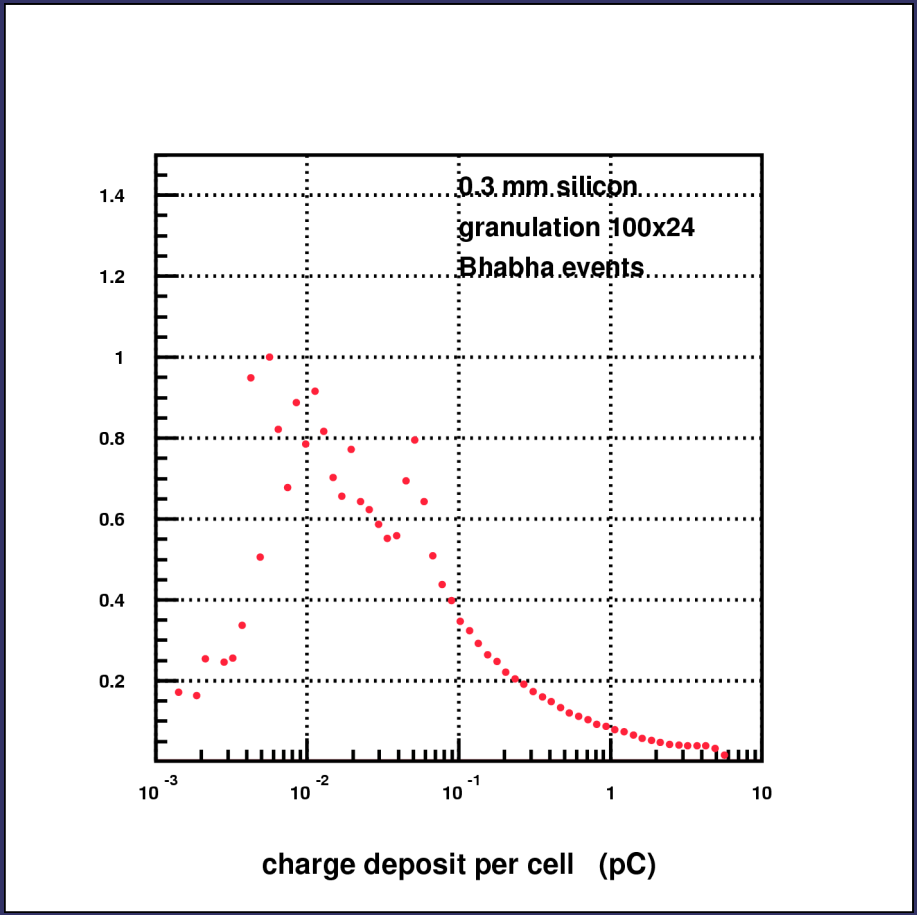
LumiCal architecture



- LumiCal ⇔ of 30 discs of silicon detectors (300 μm)
  - Disc ⇔ 24 azimuthal (15 degree) sectors
    - Sector ⇔ (R_{in}=6cm, R_{out}=35cm) built of ~100 radial pads

Specifications for front-end

- Signal: from 4fC (muons in test mode) up to ~6pC (physics mode)
- Occupancy: up to ~20% (beam-strahlung), below 1% (bhabha)
- Detectors:
  - DC-coupled 300 μm Si pads
  - C_{det} range: 20pF-120pF plus fanout (~1pF/cm ?)
  - Leakage current ?
- Inter bunch time: 330ns
- Power limitations ?



Front-end implications

Large C_{det} range

↓

Charge sensitive configuration

Q_{max} ~ 6 pC

↓

Cf ~ 6-10 pF

Test & Physics mode

↓

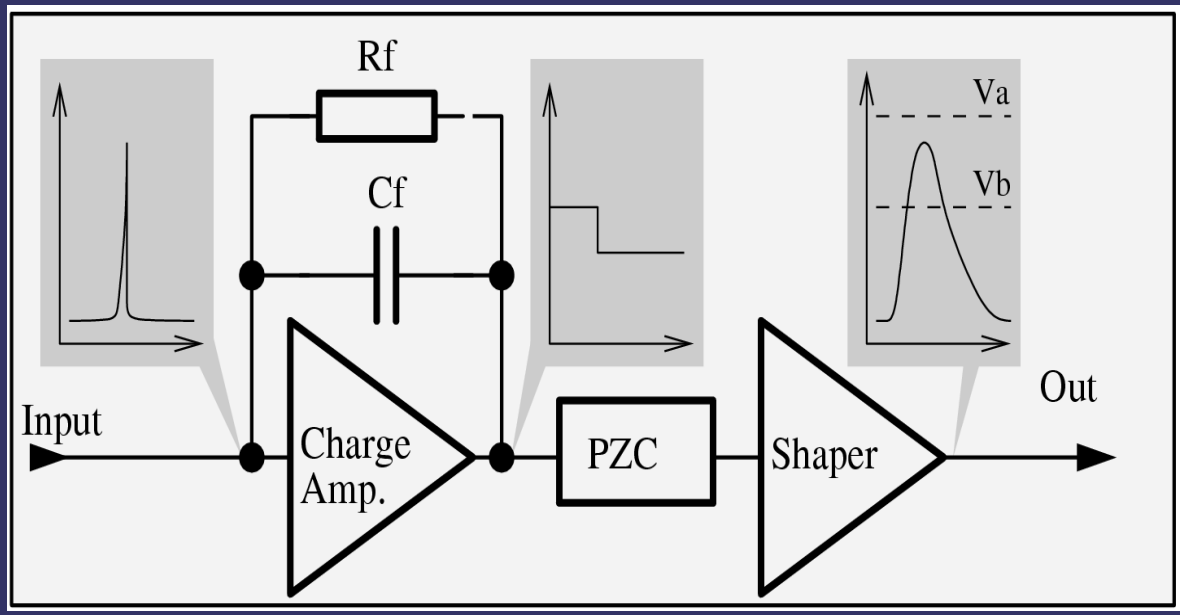
Variable gain

Δt=330 ns, pileup

↓

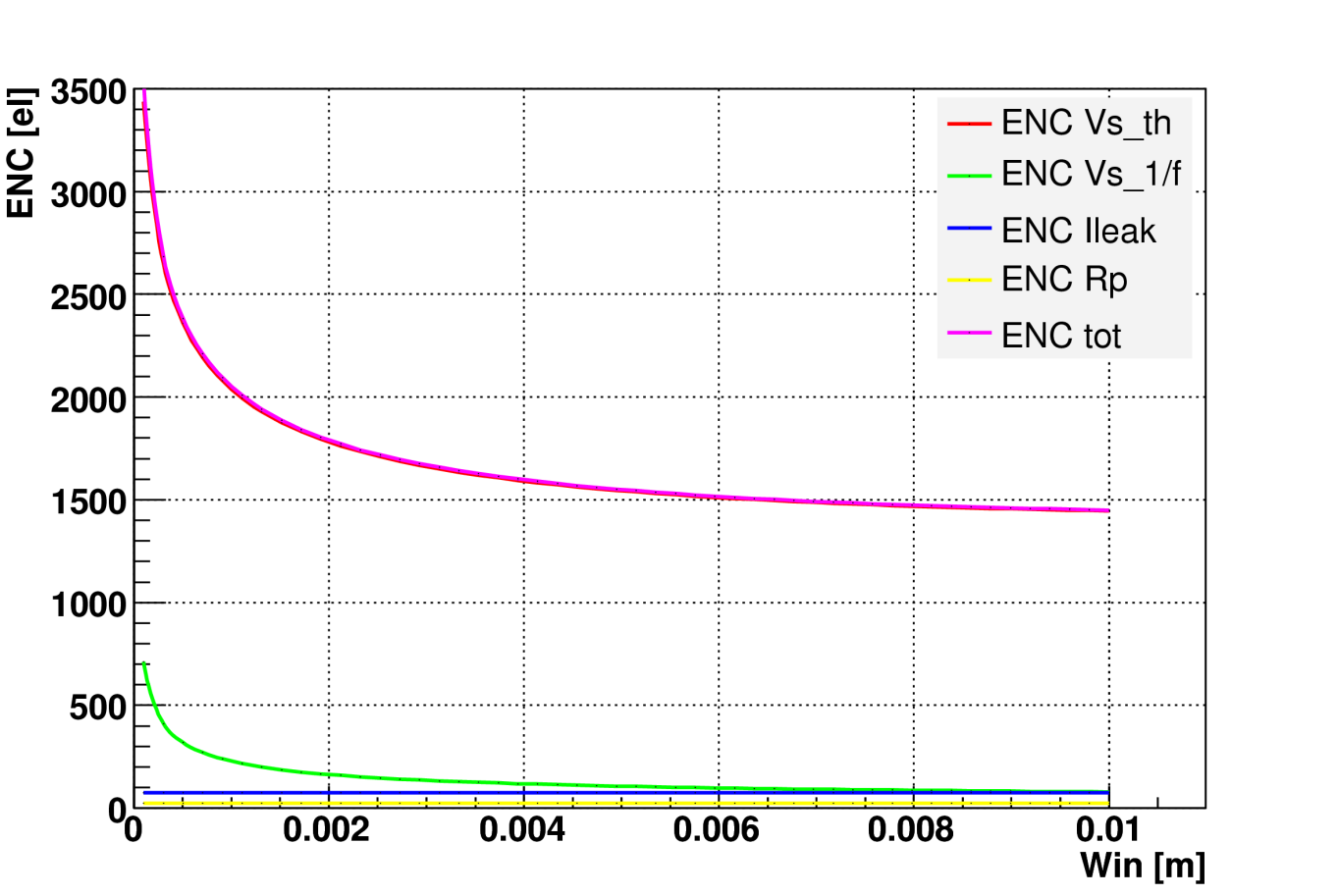
T_{peak} ~ 50-70 ns

Preamp+PZC+Shaper



Noise considerations - theory

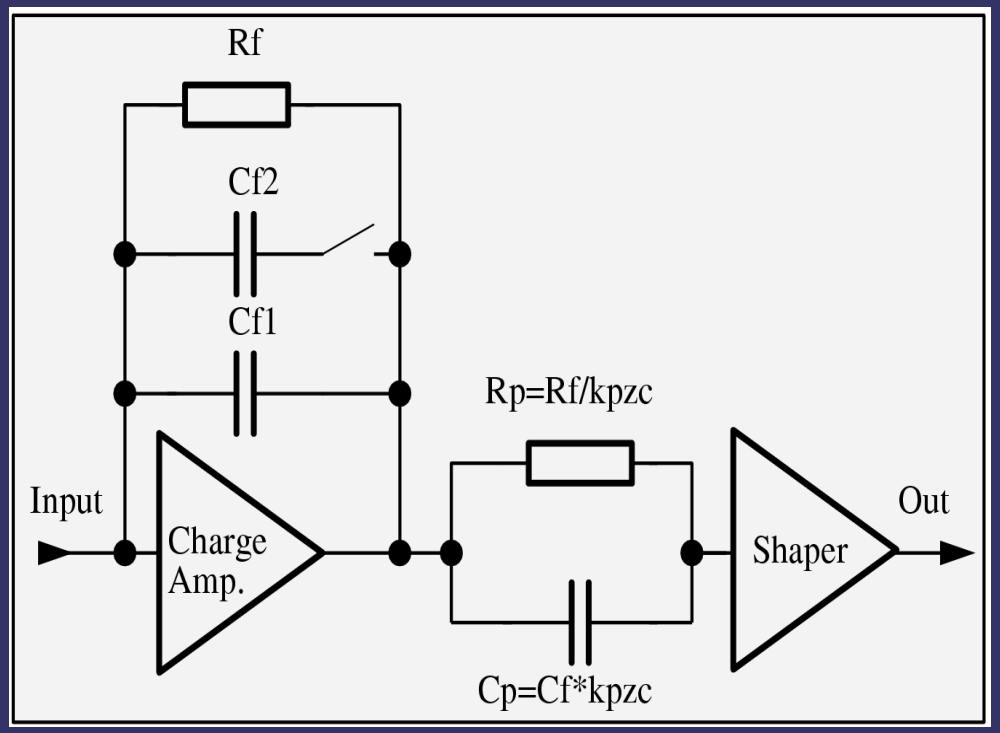
- Input stage noise (ENC) simulations with EKV model
- Assumptions: AMS 0.35 μm, C_{det}=100 pF, I=2.5 mA, 1st order shaping, T_{peak}=50ns, Rf=500kΩ, I_{leak}=10 nA



- Thermal noise dominant
- S/N=10 possible for MIP (24000el)
  - W_{in} > 2000 μm
  - I > 2mA

Front-end design

- Folded cascode amplifier
  - I~2.5mA
  - PMOS input, ~5000/0.4μm
  - Rf~500k
- Physics mode:
  - Cf=6-10pF, k_{PZC}=1
- Test mode:
  - Cf~0.5pF, k_{PZC}=10-20
- Shaper:
  - Ish~0.6mA
  - 1st order, T_{peak}=50ns
  - variable gain

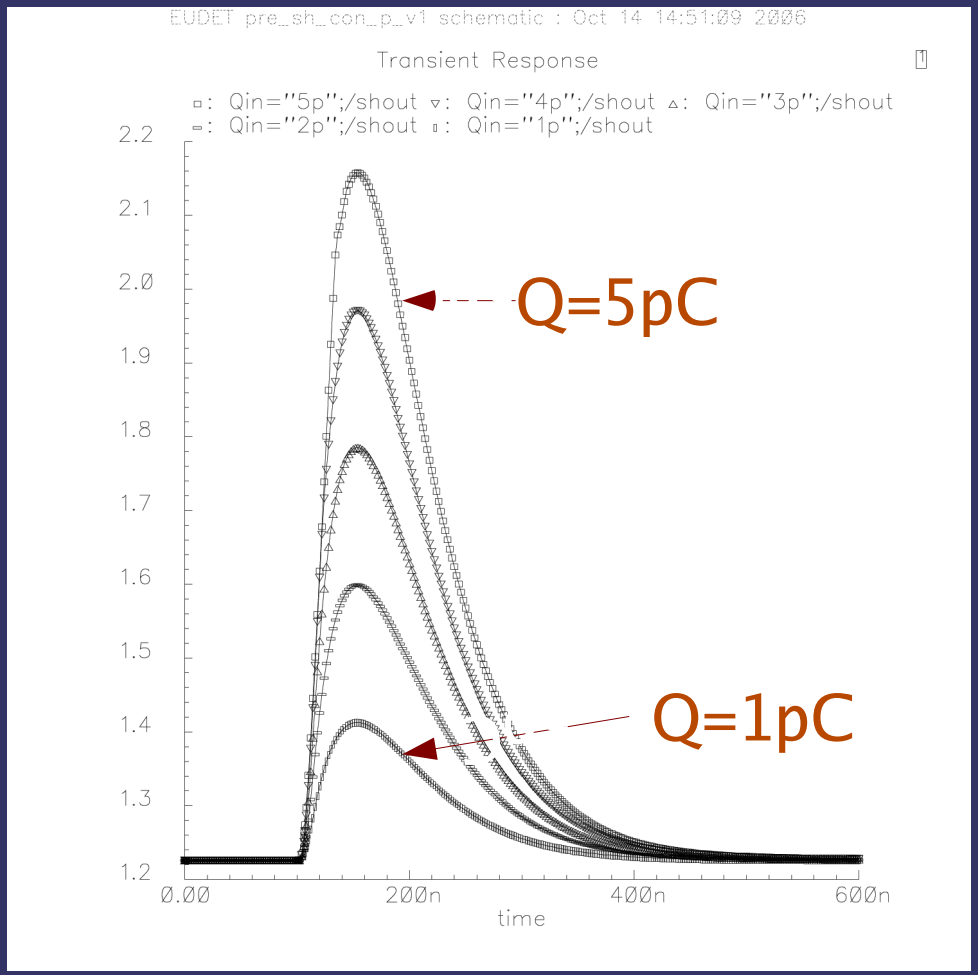


Preliminary simulations

Noise performance

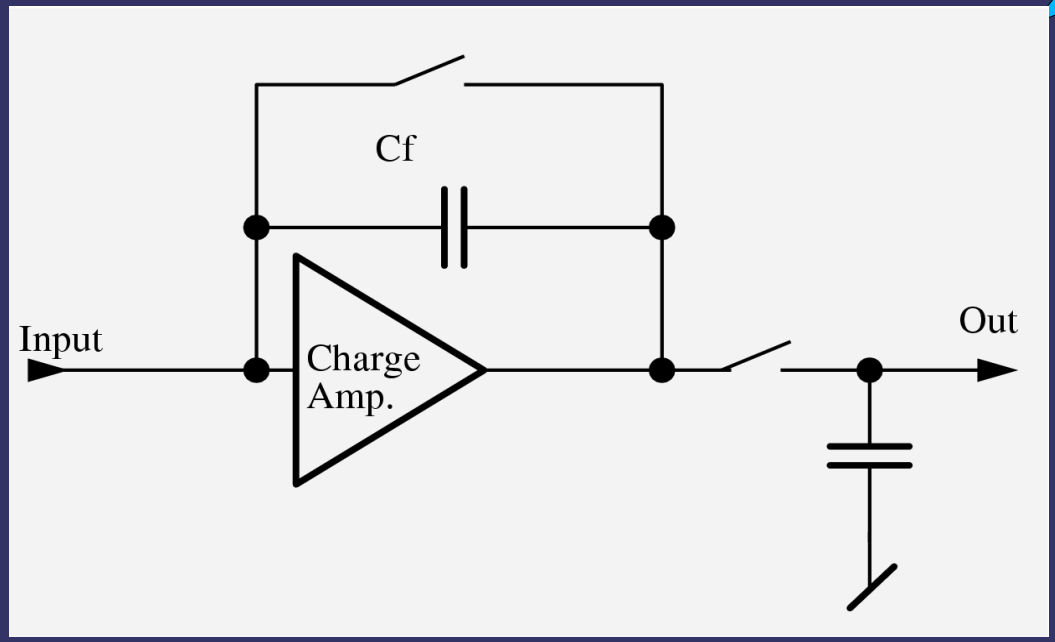
- Test mode:
  - S/N~10 (ENC~0.4 fC)
- Physics mode:
  - dynamic range > 11 bit

Linearity



Alternative front-end

Switched integrator configuration



- Simulations in progress...

Readout solutions to consider

- Is there an advantage from having a deran-domizing buffer in each channel ?
- ADC inside the chip or external ?
- Data stored in local memory during the train or sent immediately ?
- Which data protocol ?

Derandomization buffer

- Advantages:
  - Low frequency ADC/channel can be used OR high frequency ADC multiplexed to number of channels
  - Lower averaged power per channel
- Disadvantages:
  - More complicated design
  - More man power
  - Possible buffer overflow

Analog to digital converter

	External (commercial)	Internal (custom)
Need to be design	No	Yes
Space on PCB	**a lot**	No
Control	complicated	easier
Price & power	comparable	

Texas Ins.
ADS 5277

10bit, 0.9W
65MSPS, 8 chan.
$32 = 25.5 €
Tot. ≈ 20 k €

10bit, 55mW
40MSPS, 1 chan.
2.6 mm²
Tot.(P&P) ≈ 25 k €

I.Mehr and L.Singer ISSC vol. 35, pp.318, 2000

Memory and data transmission

	Test mode	Bhabha
Occupancy	5.5%	<0.2%
Direct transmission*	7.88 Gb/s	5.22 Gb/s
InterTrain transmission*	23.6 Mb/s	15.62 Mb/s
Data per Train*	7.1 Mb	4.7 Mb

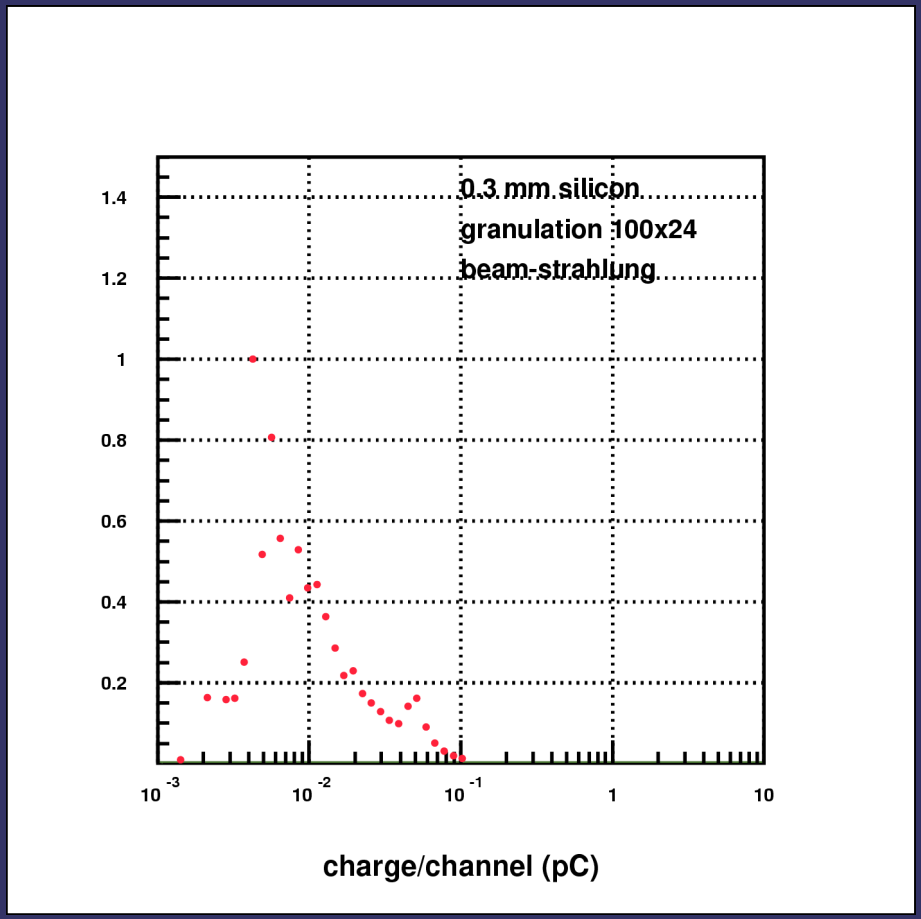
*Calculations done for half-disc unit

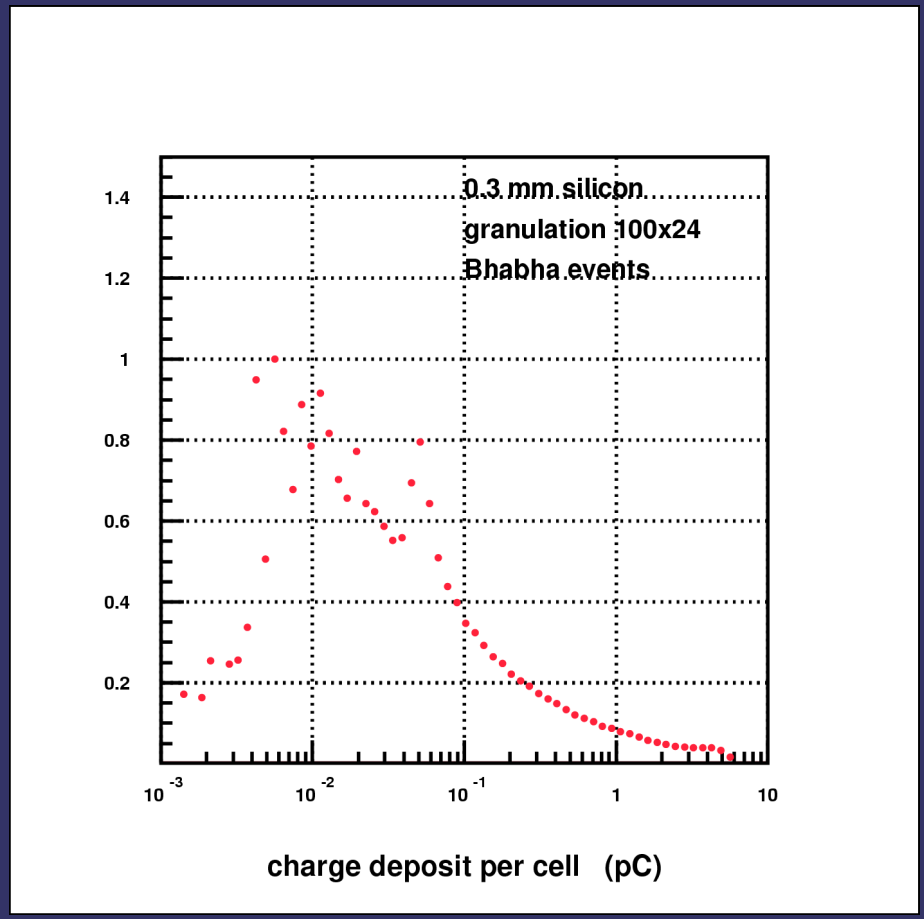
Both solutions: Direct and InterTrain transmission seem feasible
We should watch commercial solutions!

Summary & Schedule

- The work on LumiCal Readout Electronics has just started (~1 month)
- First prototypes of Front-end (and maybe something else) will be submitted in ~2-3 months
- More detailed study on Readout architecture needed (compatibility with mechanical and cooling design!)

Charge deposition





Front-end electronics