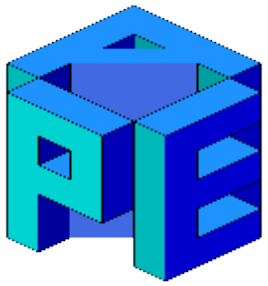
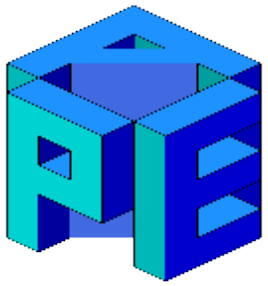


The J&T processor

- Overview of the Architecture
- Technological details
- Present status



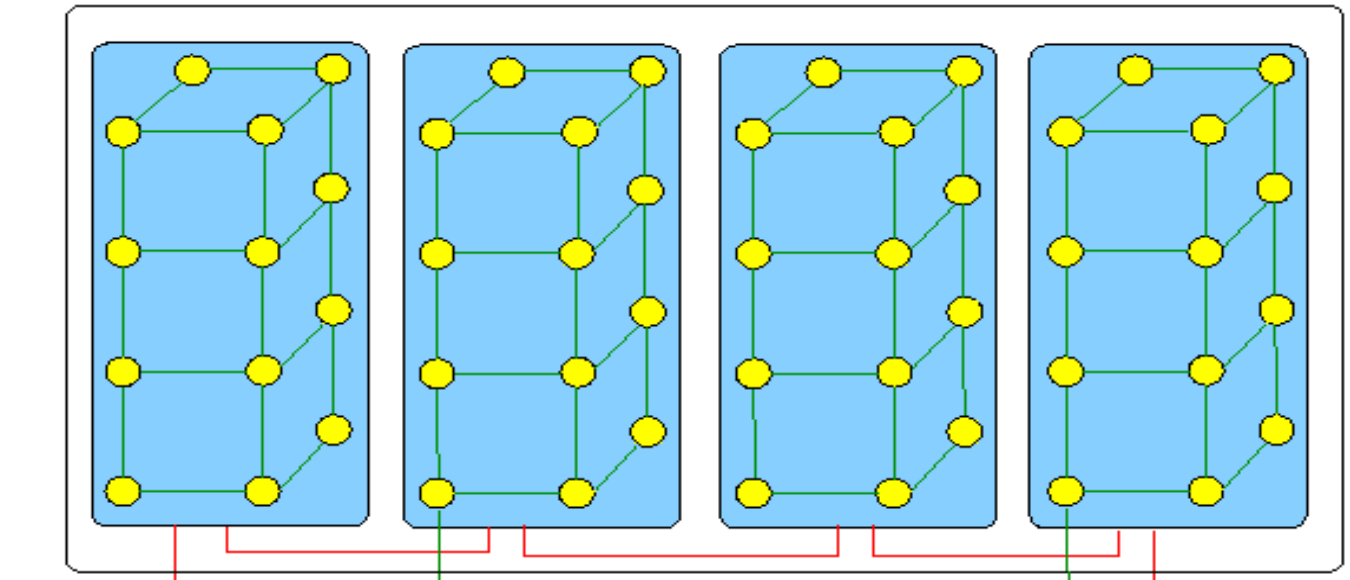
Overview of the J&TArchitecture

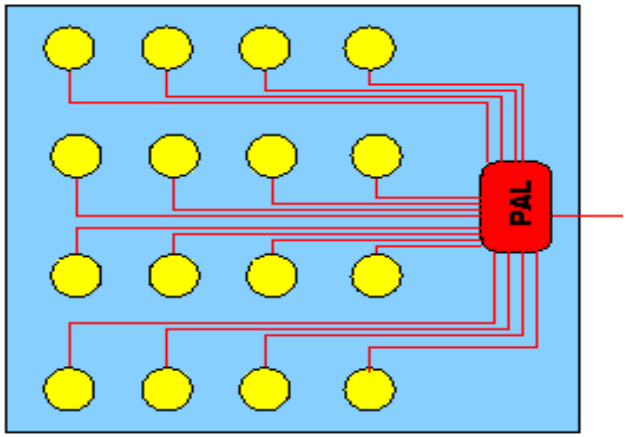
J&T is the basic (only) building block of the apeNEXT processor.
It performs several (all needed) tasks:

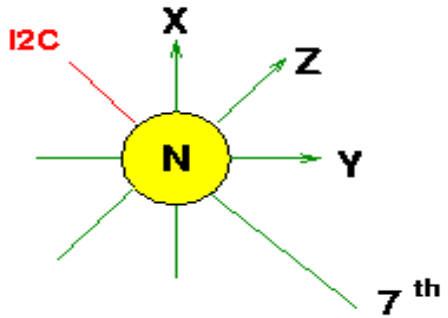
- (Mostly) floating point number crunching
- Program flow control
- Memory addressing
- Node-to-node communications (6 + 1 links)
- Slow control interface (mostly for debugging purposes)

Overview of the J&T Architecture

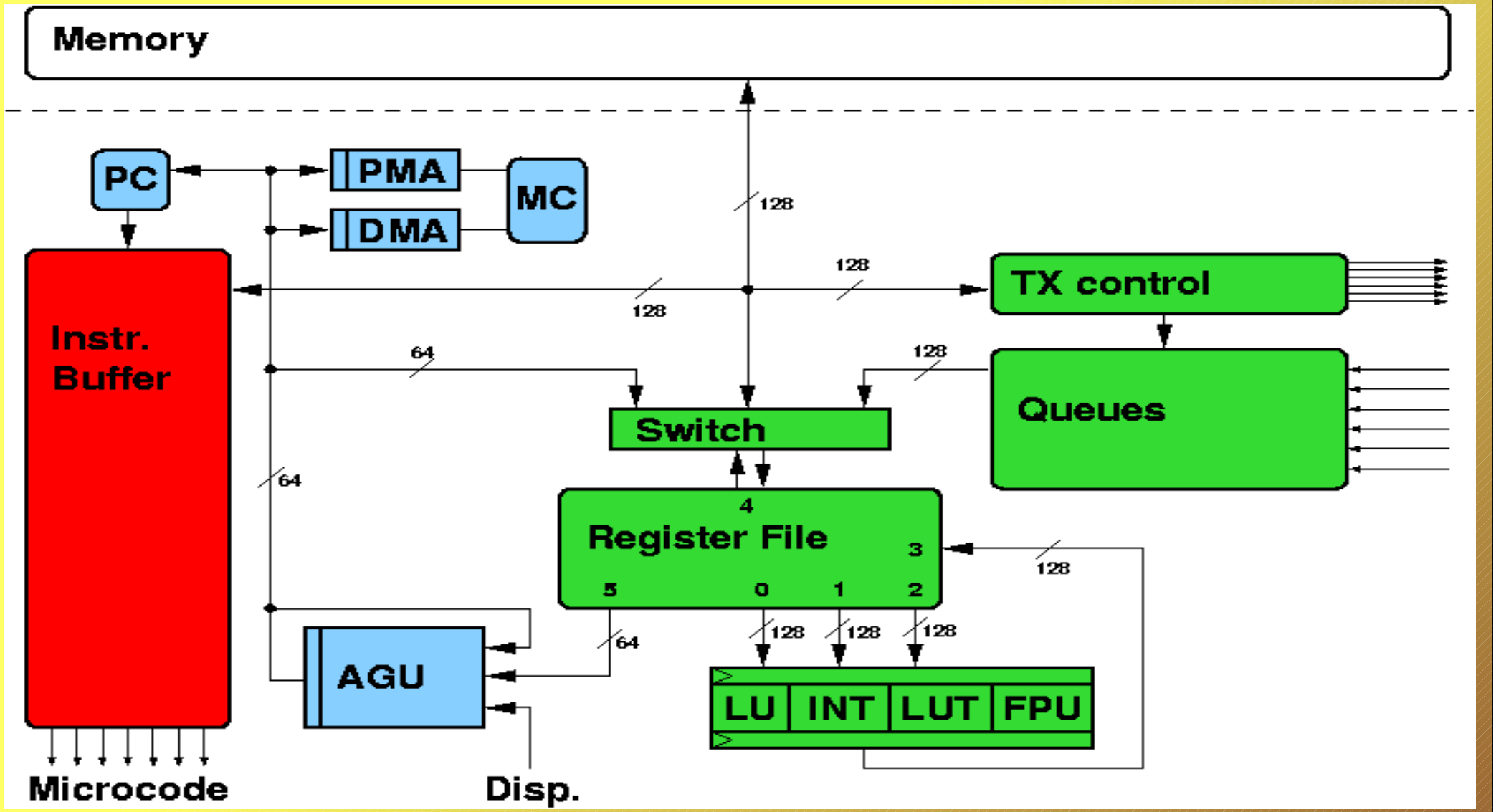
All functions required by the architecture are handled by J&T ...

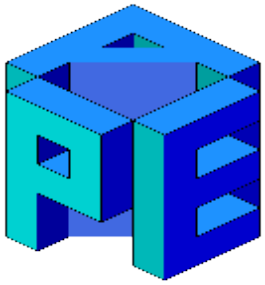






J&T: a top level block diagram

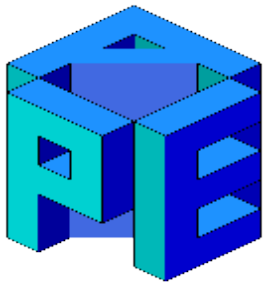




Overview of the J&TArchitecture

J&T is a technology improved replacement for the APEmille chipset (3 elements). Project goals:

- Peak floating point performance of about 1.6 Gflops (IEEE compliant double precision)
- Integer arithmetic performance of about 400 Mips
- Link bandwidth of about 200 Mbyte/sec each (full duplex)
- Support for current generation DDR memory
- Memory bandwidth of 3.2 Gbyte/sec (400 Mword/sec)

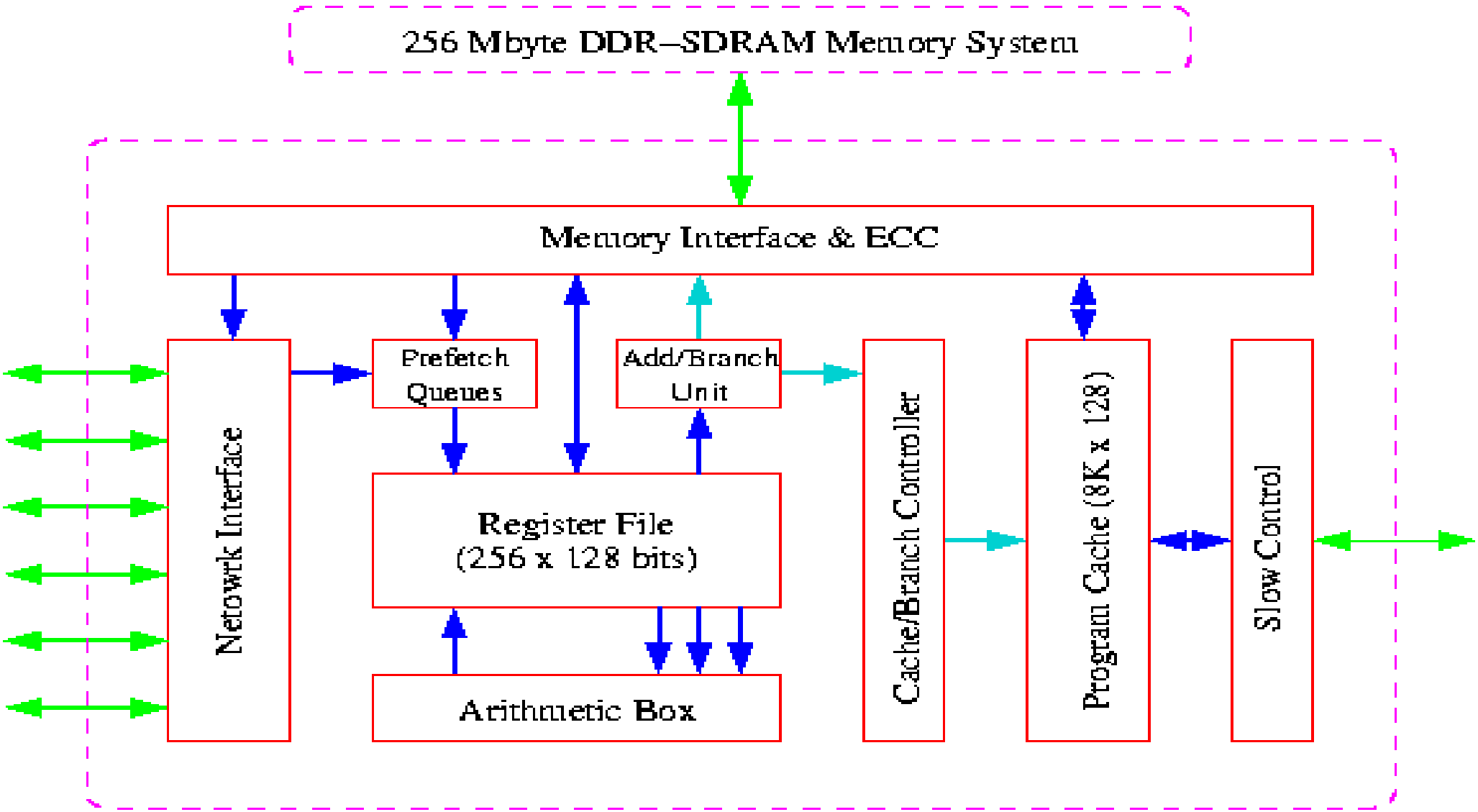


Overview of the J&TArchitecture

Changes w.r.t APEmille are dictated by technology constraints:

- Common program/data memory => Program cache/fifo
- Large memory latency => Data prefetch queues
- Hi clock frequency => Independent flow control
- Hi clock frequency => Self synchronizing nodes
- Hi clock frequency => Self-clocked link
- Memory bandwidth of 3.2 Gbyte/sec (400 Mword/sec)

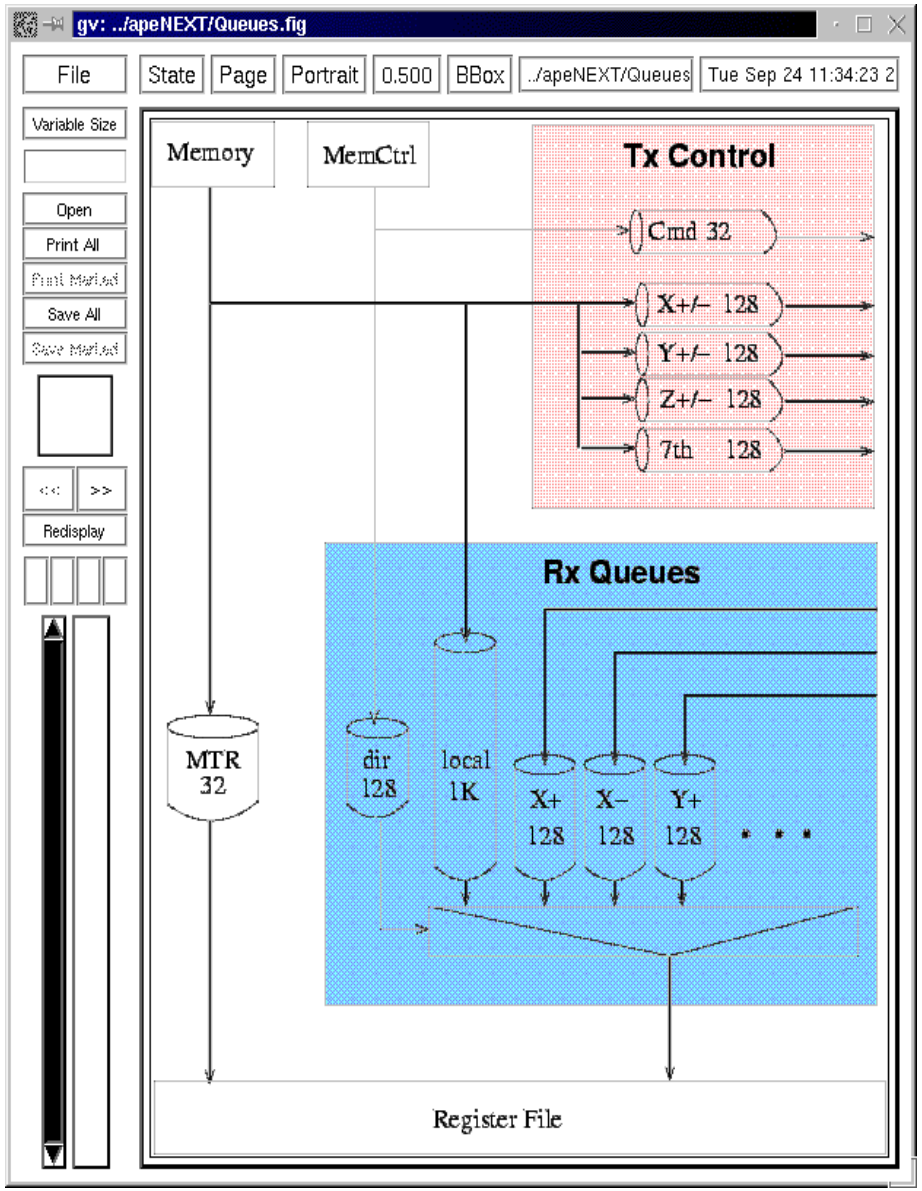
Overview of the J&TArchitecture

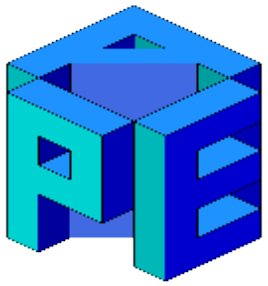


Overview of the J&TArchitecture

Selected highlights: the Memory queue

- Local prefetch queue (replace cache)
- Remote prefetch queue
- Automatic reordering of arriving packts.

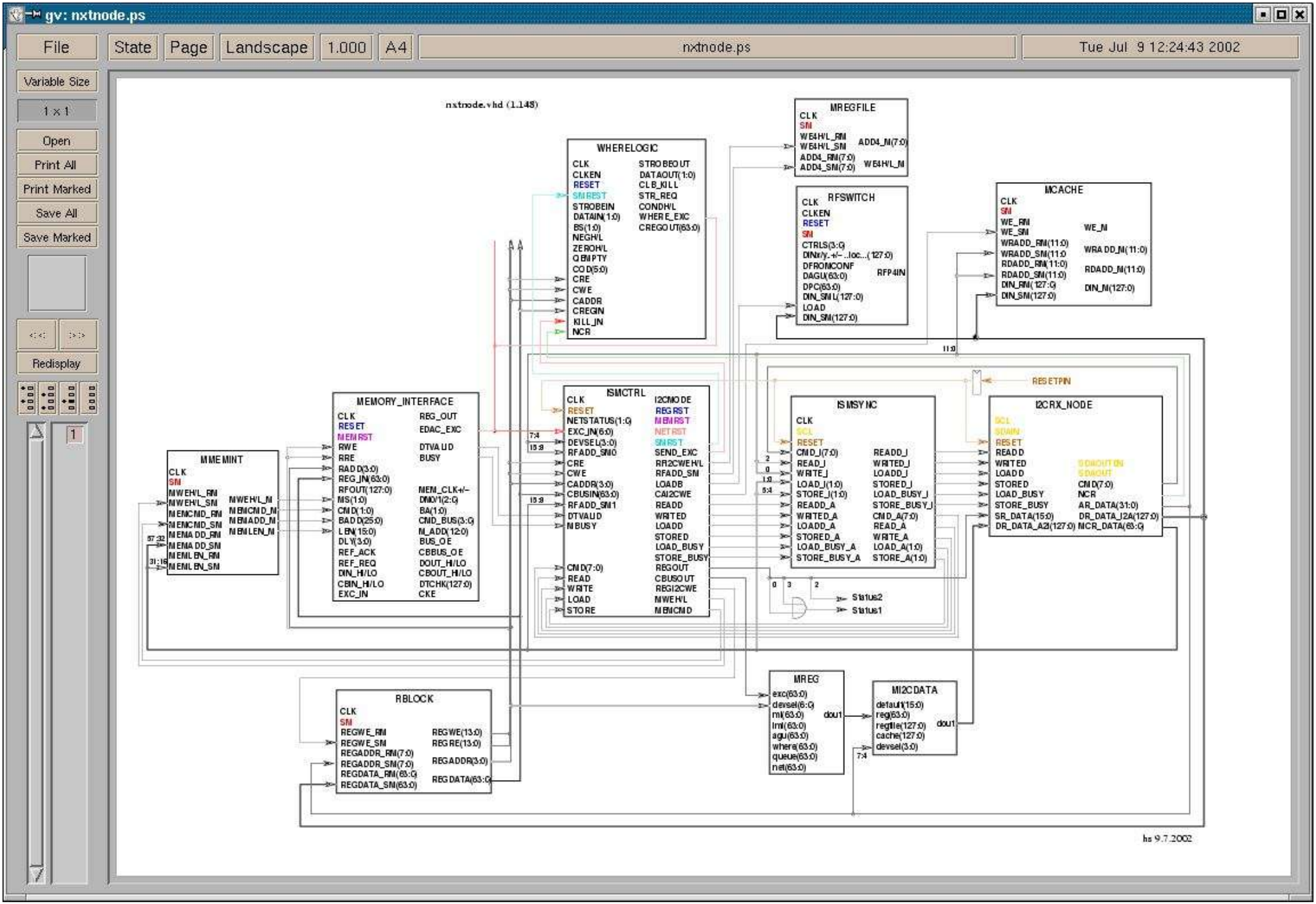




Overview of the J&TArchitecture

The processor design is based on:

- VHDL description of the system (~55000 VHDL lines)
- Synopsys based synthesis on a CMOS technology
- + Memory macrocells
- Synopsys based placement (Physical compiler)
- Cadence based routing (SE) and back-annotation
- Mostly functional test-vectors
- Limited use of TetraMax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MREGFILE
RFSWITCH
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MMEMINT
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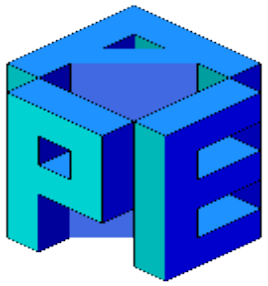
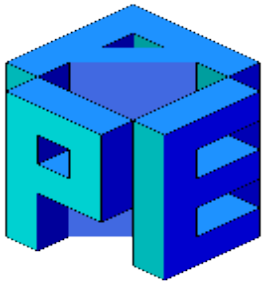


Overview of the J&TArchitecture

Some figures concerning the physical implementation:

- 0.18 micron/5metal(Al) CMOS technology by Atmel
- 450 signal pins
- 600 total pins (Bga package)
- LVDS (differential) signalling for communication links
- SSTL signalling for DDR memory interface
- 16.0 x 16.0 mmsq (heavily pad limited)
- 5.0 Watt estimated power at 200 Mhz

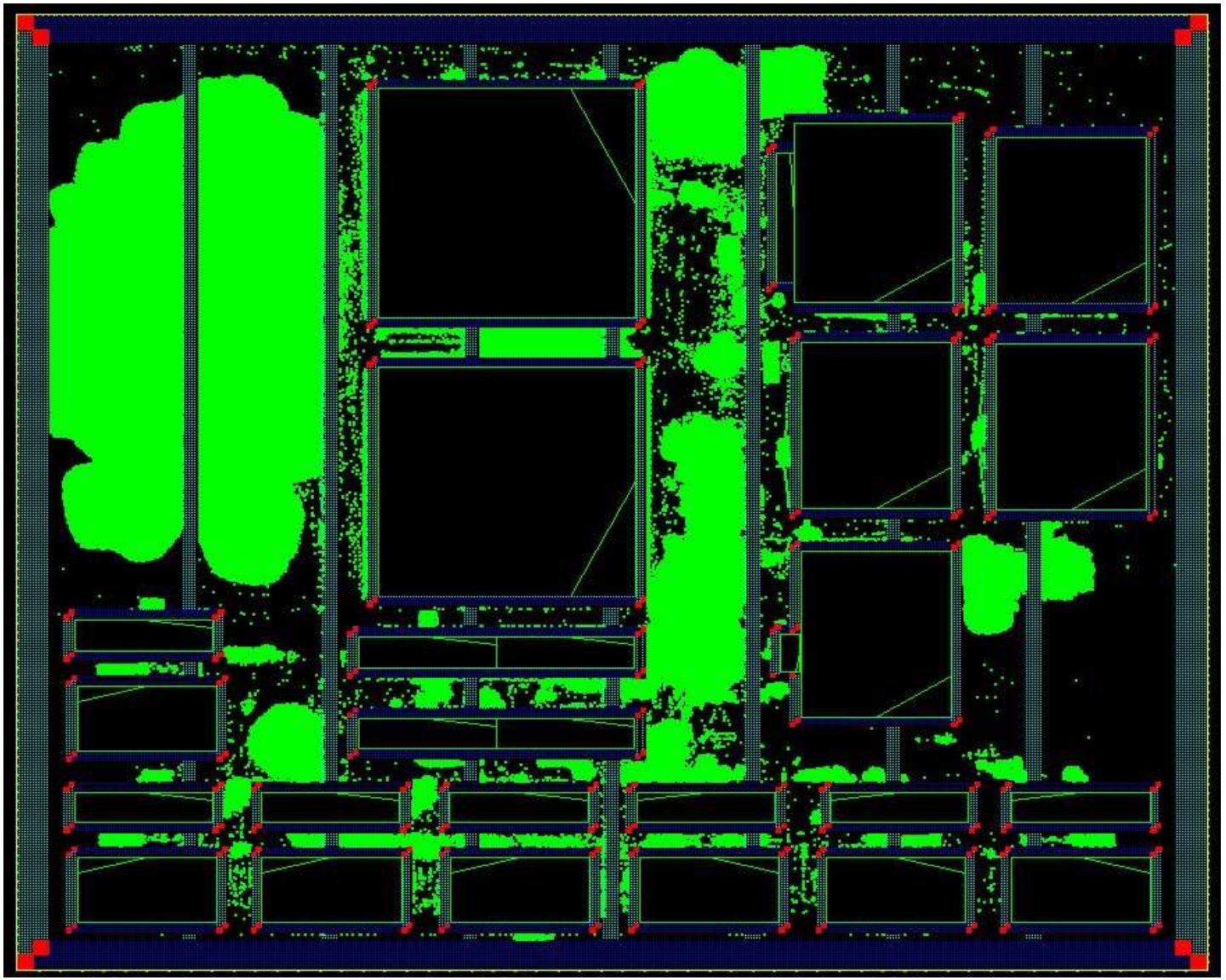


Overview of the J&TArchitecture

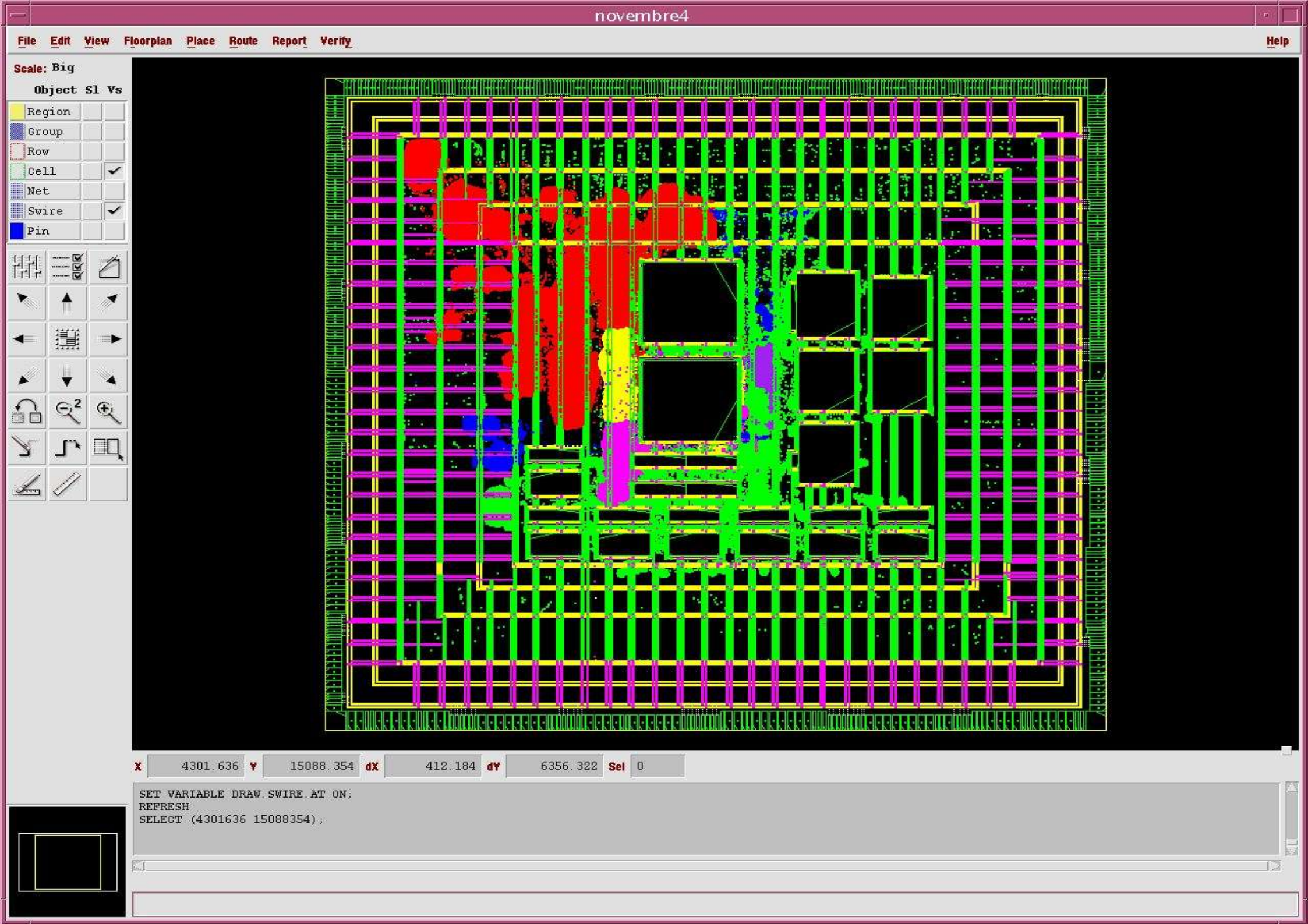
Some more figures concerning the physical implementation:

- Approx. 20 mmsq memory macrocells
- Approx. 520K equivalent gates random logic
- Number crunching: 160K
- Register file: 240K
- Glue logic: 120K
- 450 signal pins
- 600 total pins (Bga package)
- 16.0 x 16.0 mmsq (heavily pad limited)
- 5.0 Watt estimated power at 200 Mhz

Placement problems



Power Distribution was grossly understimated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File
Edit
View
Floorplan
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Report
Verify
Help
Scale: Big
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Row
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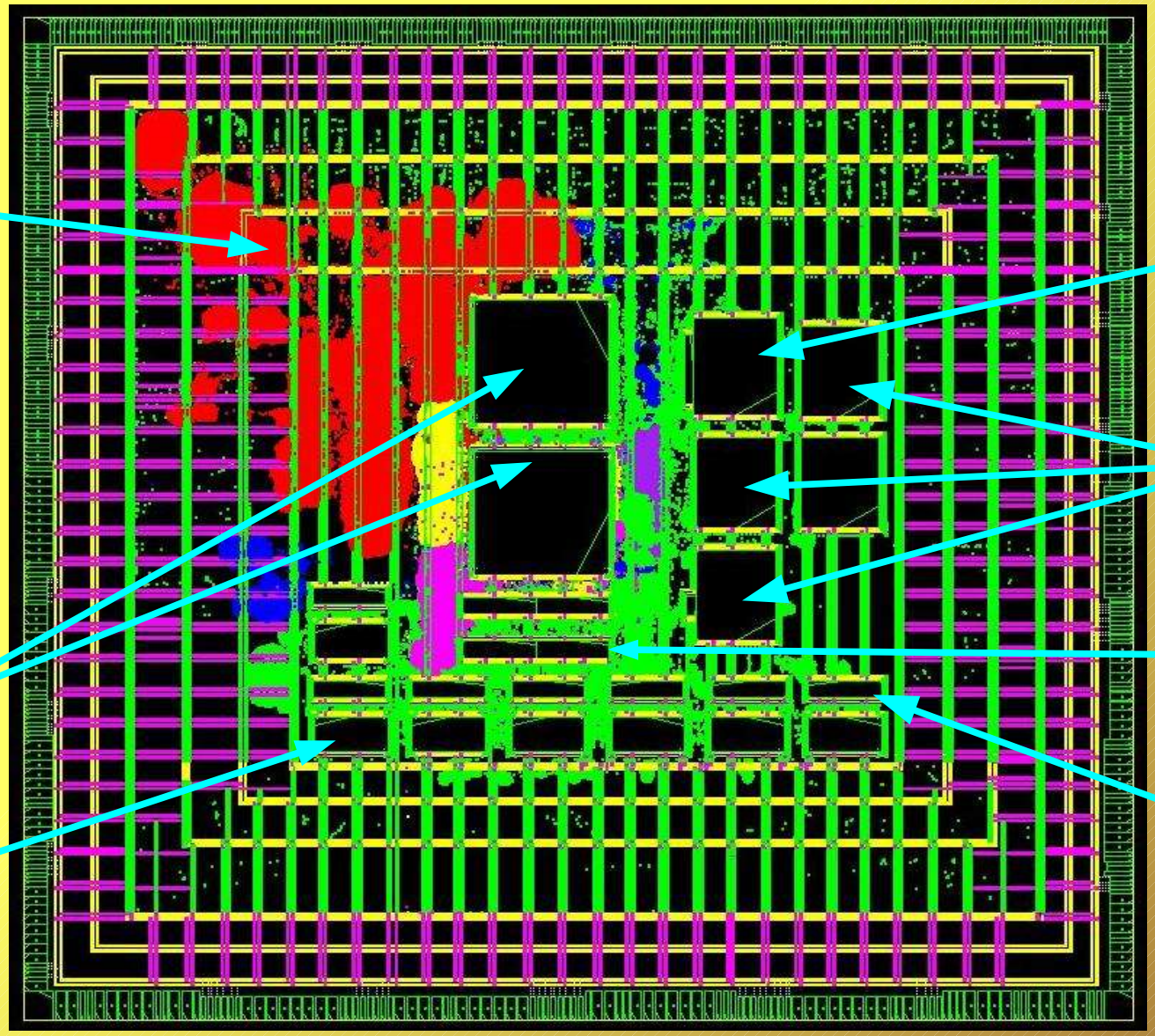
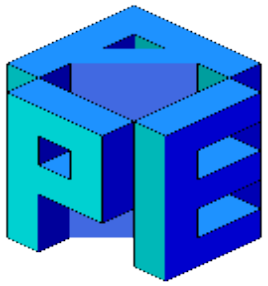
Swire
Pin
X 4301.636 Y 15088.354 dX 412.184 dY 6356.322 Sel 0
SET VARIABLE DRAW.SWIRE.AT ON;
REFRESH
SELECT (4301636 15088354);

Floorplanning ....





Where are why today

- Design completed around July 20th, 2003
- Back-end completed by Atmel around Sept. 10th 2003.
- Protos delivered by Sankta Klaus
- Functional tests started around January 10th
- 'large' application cores running after just a few days
- Crossing fingers.... everything logically OK
- Have to measure actual operating frequency (< 200 Mhz)

Photo Gallery: proto #1

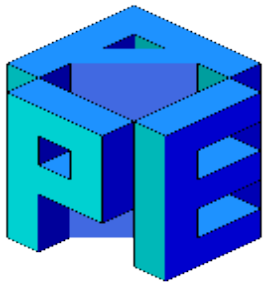


Photo Gallery: apeNEXT module

Photo Gallery: testing # 1

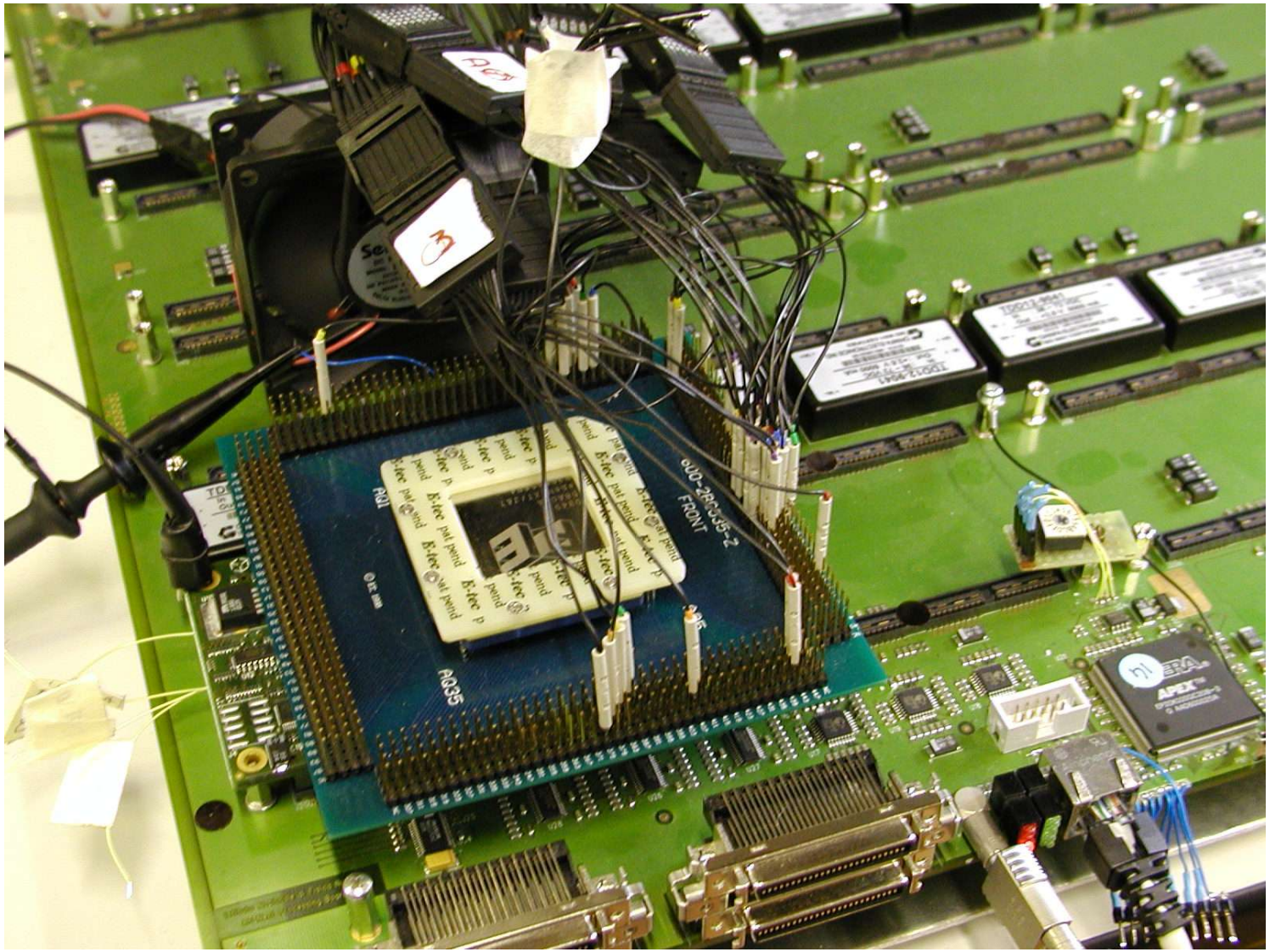


Photo Gallery: processing Board

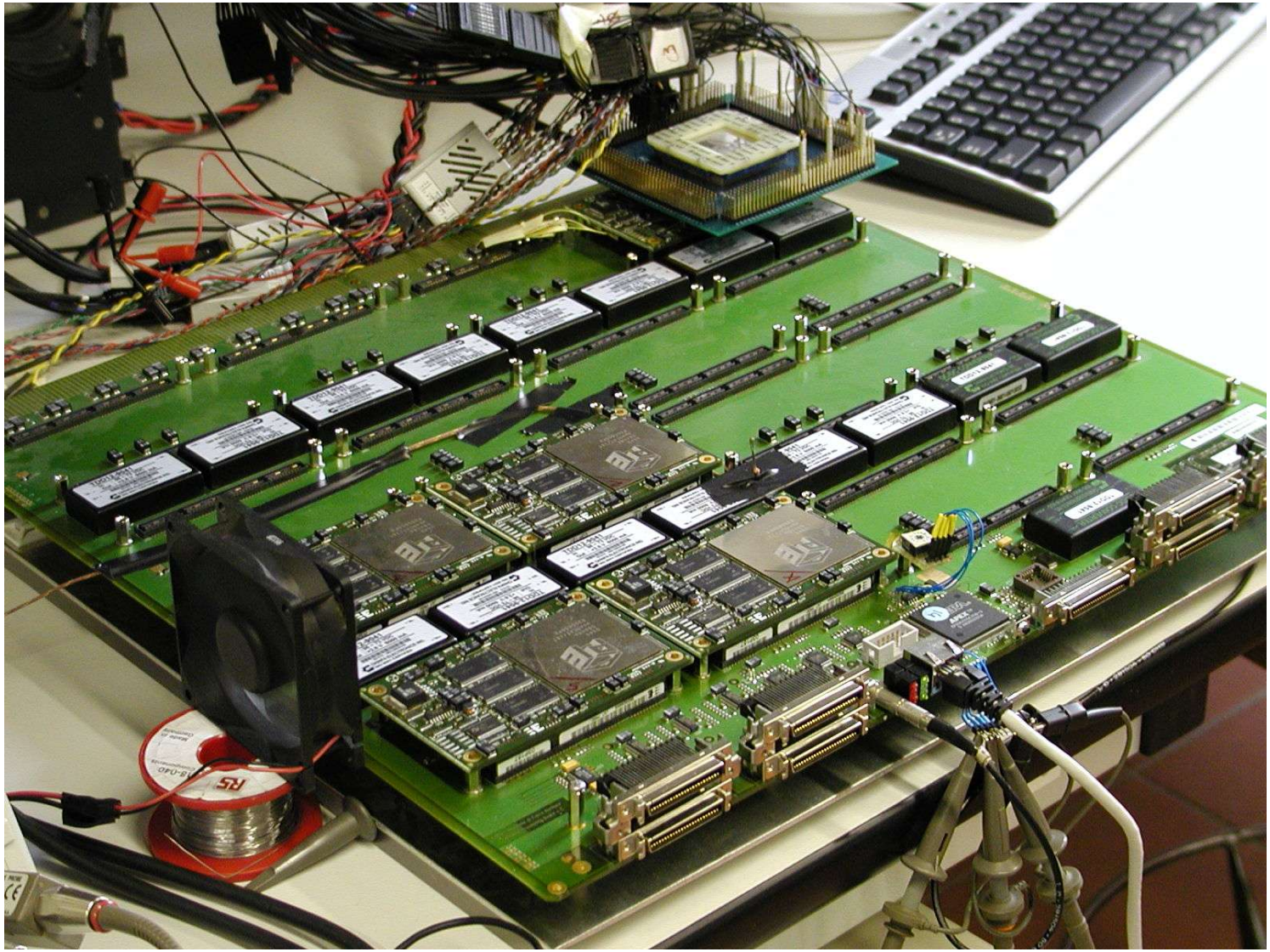


Photo Gallery: the 'eyes' of the LVDS link

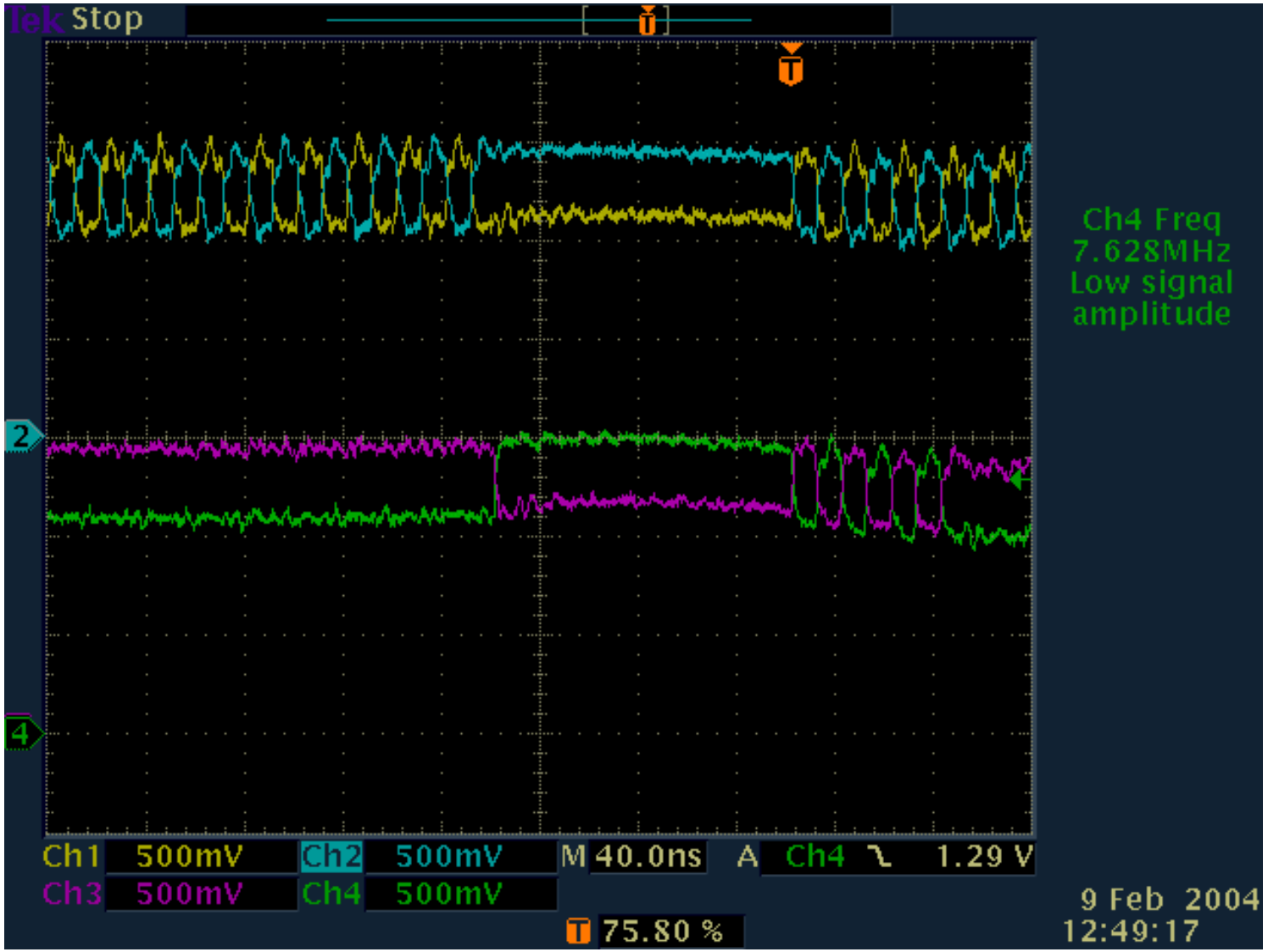
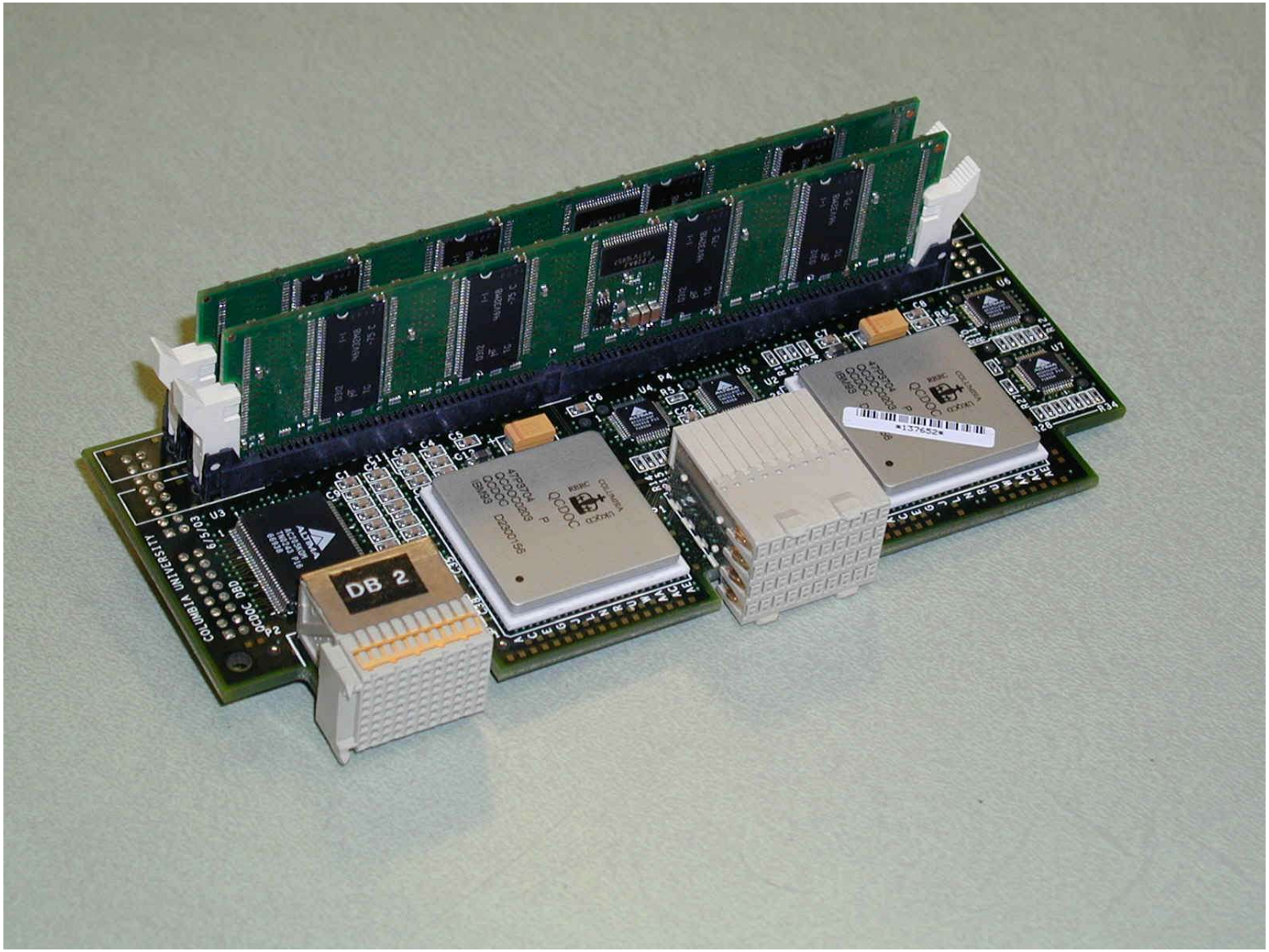
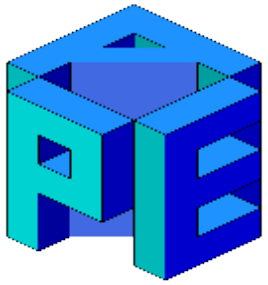


Photo Gallery: our competitors

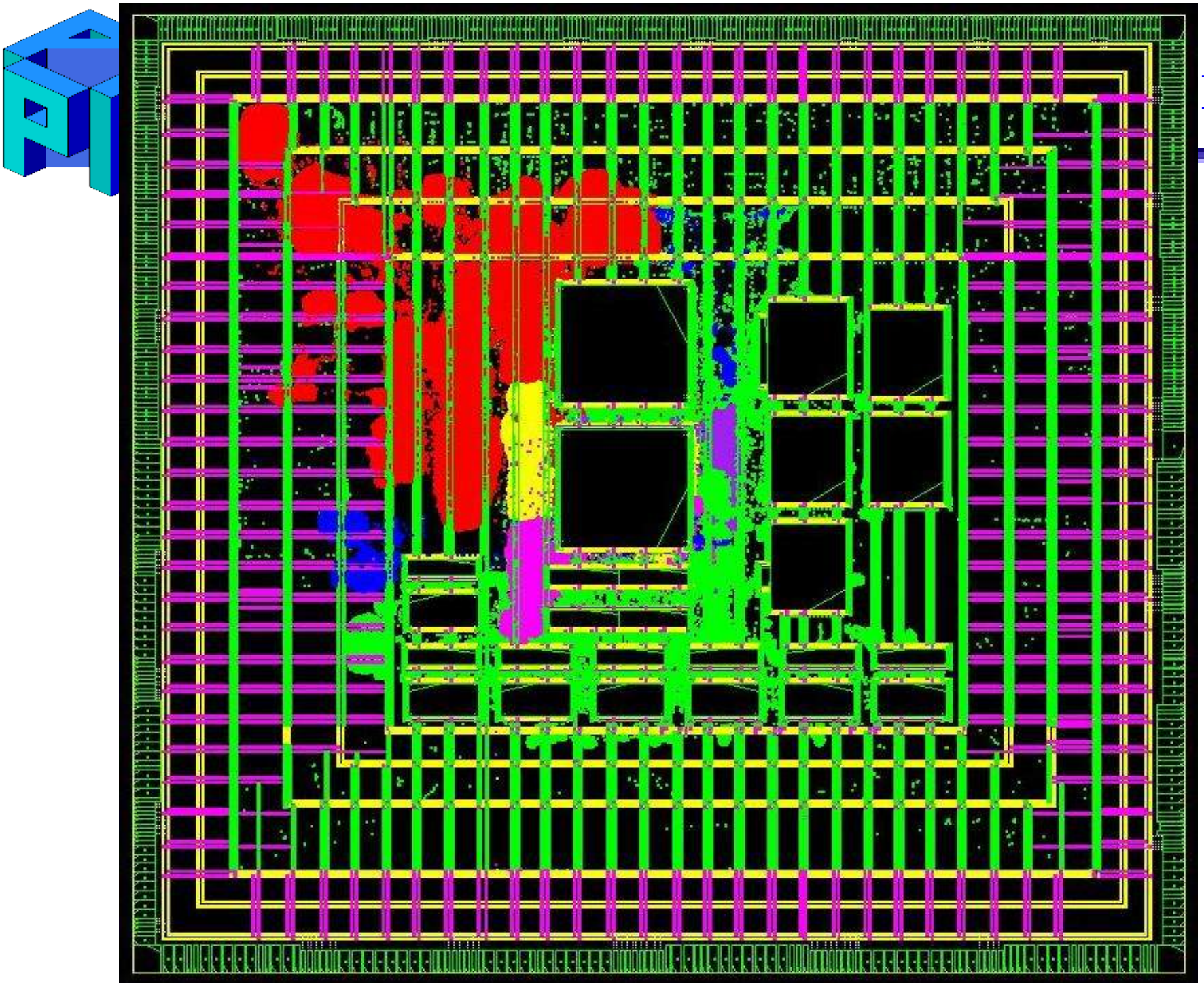




Alist of errors (with hindsight...)

Shouldwe restart the project today from scratch (which we will NOT do), we would:

- Reduce glue-logic complexity (even more focus)
- Reduce the size of the fastest clock partition
- Start placement at an erlier step
- Select a different silicon foundry (confidential)



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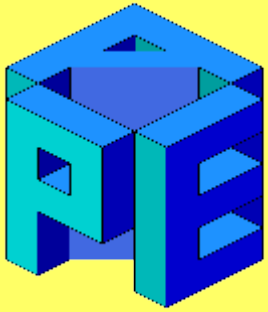

The arithmetic unit

Performance Estimates (clock cycle of 5 ns):

Type	Performance	Operands in RF	Latency (clock cycles)
Complex	1600Mflops	256	10
Real	400Mflops	512	7
Real. vect	800Mflops	256	7
Integer	200Mips	512	4
Int .vect	400Mips	256	4