Pair Monitor Studies

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We study for the pair monitor which measures the beam profile at the interaction point by using the distribution of e^+e^- pair generated from the beam crossing. The simulation study confirmed that the pair monitor can measure the vertical beam size with 8% level with the e^+e^- distributions accumulated for 150 bunches. As the hardware study, the readout ASIC is developed. The shift register to specify the readout cell was verified to work correctly.

1 Introduction

The pair monitor is used to check the beam profile at the interaction point (IP), measuring the distribution of the e^+e^- pairs generated during beam crossing [2]. The particles of concern have the same charge as that of the oncoming beam, and are hereafter called "same-charge" particles. Most of them are deflected at larger angles than their inherent scattering angles by a strong electromagnetic force due to the oncoming beam, while the "opposite-charge" particles must oscillate inside the oncoming beam because of a focusing force between them; they are deflected with small angles. They can be well described by a scattering process of $e^-(e^+)$ in a two-dimensional Coulomb potential that is Lorentz boosted to the rest frame of the oncoming beam. Since this potential is produced by the intense electric charge of the oncoming beam, it is a function of the transverse size (σ_X, σ_Y) and intensity of the beam. Therefore, the deflected particles should carry this information, especially in their angular distribution. The pair monitor uses this principle to extract information of the beam profile at IP.

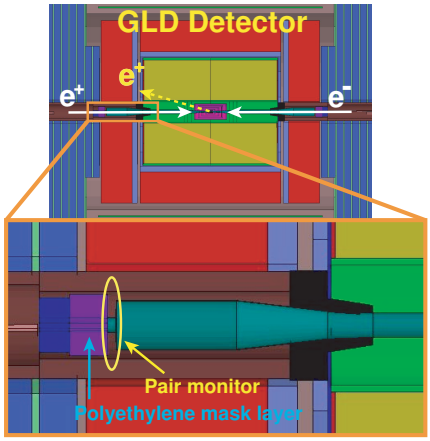

Figure 1: The simulation setup. The pair monitor is located at 400 cm from IP, that is in front of the Polyethylene mask layer.

We study the pair monitor to be used for the ILC beam profile monitor. The performance check and its optimization are performed by the simulation. In addition, we develop a readout ASIC suitable for the pair monitor. In this paper, the current status of these studies are reported.

2 Simulation Study

The performance and optimization of the pair monitor is studied with the simulator based on the Geant4, which is used for the GLD detector (Jupiter). In the simulation, e^+e^- events from the beam crossing are generated by CAIN, in which the standard beam size is defined as $(\sigma_X, \sigma_Y, \sigma_Z) = (639$ nm, 5.7 nm, 300 μm). Figure 1 shows the simulation setup. The pair monitor is located at 400 cm from IP, that is in front of the Polyethylene mask layer to absorb γs and $e^{\pm}$s created in the BCAL. The magnetic field is set to 3 T with anti-DID.

In this study, the e^+e^- distribution is studied at the left side in Figure 1, where the oncomming beam is e^+. Therefore, e^+ distributions on the pair monitor have the beam information, since e^+ is scattered with large angle whereas the e^- is not scattered so much.

As the first step, the performance to measure the vertical beam size is checked. Figure 2 shows the relation between r and ϕ for e^+, where r is the radius from the center of the extraction beam pipe for the e^- beam and ϕ is the angle around it. We select the L-region ($\phi = -3.14 \sim -1.8$ rad. and $r = 2 \sim 7$ cm) and H-region ($\phi = -1.4 \sim 2.5$ rad. and $r = 2 \sim 5$ cm) as shown in Figure 2, where the number of events depends on the vertical beam size largely. In the L-region, the number of the events decreases for larger vertical beam size, and that increases in the H-region. To extract information of the beam size, the peak-to-valley ratio is defined as N_L/N_H, where N_L and N_H are the number of events in the L-region and H-region, respectively. Changing the vertical beam size, we compare the peak-to-valley ratio.

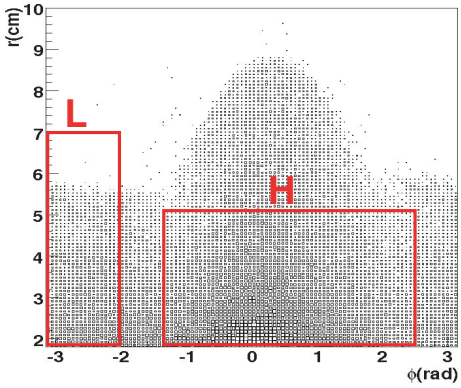

Figure 2: r v.s. ϕ distribution for e^+, where r is the radius from the center of the extraction beam pipe for the e^- beam and ϕ is the angle around it.

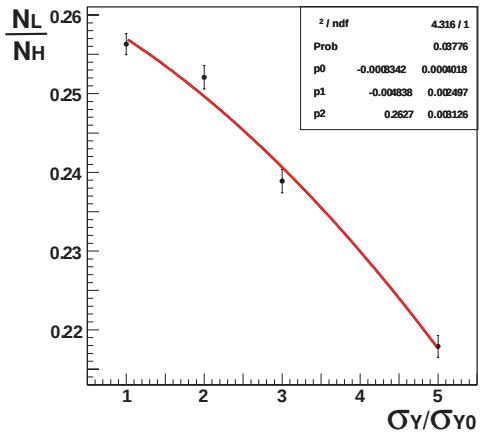

Figure 3: Peak-to-valley ratio as a function of the ratio between the vertical beam size used in the simulation (σ_Y) and the standard vertical beam size ($\sigma_{Y0} = 5.7$ nm).

Figure 3 shows the peak-to-valley ratio as a function of the ratio between the vertical beam size used in the simulation (σ_Y) and the standard vertical beam size ($\sigma_{Y0} = 5.7$ nm). To make the figure, data for 21, 26, 27, and 50 bunches is accumulated for the vertical beam size of σ_{Y0}, $2\sigma_{Y0}$, $3\sigma_{Y0}$, $4\sigma_{Y0}$, and $5\sigma_{Y0}$, respectively. In Figure 3, the statistical error is assigned to the error bar. The peak-to-valley ratio depends on the vertical beam size clearly.

The performance to measure the vertical beam size is investigated when the data is

accumulated for 150 bunches. The statistical error in Figure 3 is scaled to that for 150 bunches. Then, it is transformed to the uncertainty of the horizontal axis by using the fitting function obtained in Figure 3, that corresponds to the measurement accuracy of the vertical beam size. As the result, 8% accuracy is obtained when the vertical beam size is the standard one.

3 Development of Readout ASIC

We develop the readout ASIC for the pair monitor. It is designed to count a number of the hit to obtain the hit distribution on the detector. The statistics for about 150 bunches is enough to extract the beam information from the simulation study. Therefore, the number of the hit is counted for 16 timing parts in one train, which corresponds to 167 (= 2670/16) bunches in the current nominal ILC design. The hit counts for each timing parts are read within the timing width between each train (200 ms). A silicon pixel sensor with the thickness of about 200 μm is assumed as a detector candidate, whose signal level is about 15,000 electrons. The readout ASIC is designed to satisfy these concept.

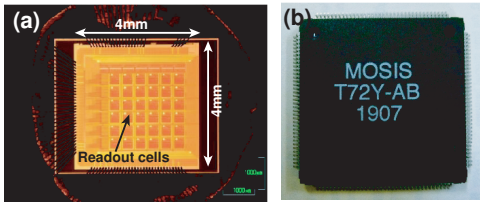

Figure 4: A prototype of the readout chip: (a) before package (b) after package.

The readout ASIC consists of the distributor of the operation signals, shift register to specify a readout cell, data transfer to the output line, and 36 readout cells. A readout cell consists of the amplifier, comparator, 8-bit counter, and 16 count registers. They are aligned to 6×6 for the X and Y directions. The prototype AISC was produced with 0.25 μm process. Its layout was made by Digian Technology, Inc. [3], and the production was done by the MOSIS Service [4]. The chip size is 4×4 mm^2, and the readout cell size is 400×400 μm^2. To test the response of the readout chip, it is covered with MQFP package produced by I2A Technologies [5].

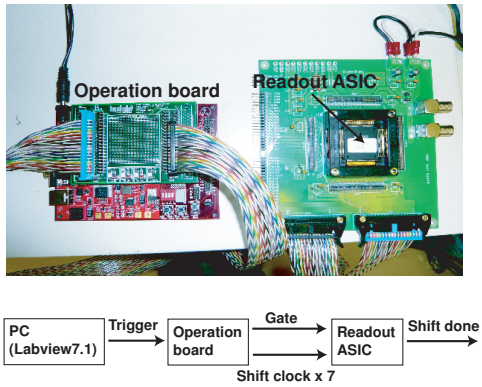

Figure 5: Experimental setup for the response test of the readout ASIC.

As the first test, the response of the shift register was checked. The shift register is used for the specification of the readout cells. The specification is done by inputting the shift clocks for the X and Y direction when the enable gate is opened. At the timing of the seventh shift clock for the X or Y directions, the shift register is designed to output the shift-done signal. Therefore, the response of the shift register can be confirmed by checking the shift-done signal after inputting the 7 shift clocks to one direction.

Figure 5 shows the experimental setup for the response test of the readout ASIC. The

trigger signal is sent to the operation board (Spartan3 starter kit) from a computer, whose operation is done by using LABVIEW 7.1. The operation board is mounted a FPGA (Field Programmable Gate Array) which realizes flexible modification of the logic. An enable gate and shift clocks are sent to the readout ASIC by the operation board. The shift-done signal is monitored by an oscilloscope.

The first prototype is produced in 2005. The shift-done signal is output without regard to the timing of the shift clock. After the investigation, all the digital inputs were insulated by mistake in the production of the prototype. Therefore, the digital input was short-circuited in the second prototype, which was produced in 2007.

Figure 6 shows the test result of the shift register for the second prototype. We can see the shift done-signal at the timing of the seventh shift clock. From this result, it is confirmed that the shift register works correctly.

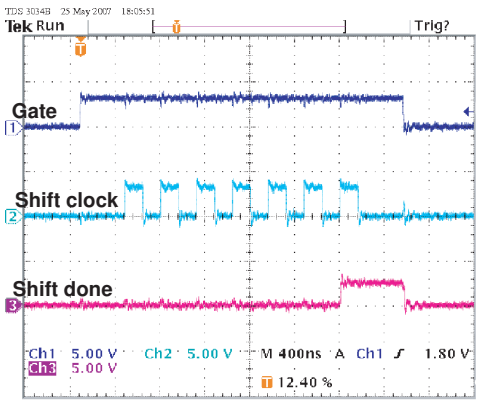

Figure 6: The test result of the shift register for the second prototype. The shift-done signal is output at the timing of the seventh shift clock.

4 Conclusions

We study the detector optimization and the readout ASIC for the pair monitor. The simulation study confirmed that the pair monitor can measure the vertical beam size with 8% level with the e^+e^- distributions accumulated for 150 bunches. The readout ASIC is developed for the pair monitor. Although the digital input was insulated in the first prototype, it was modified for the second prototype. The shift register to specify the readout cell was verified to work correctly.

5 Acknowledgments

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